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Heuristic Detection of the Most Vulnerable Regions in Electronic Devices for Radiation Survivability

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As electronic systems become larger and more complex, detection of the most vulnerable regions (MVR) to radiation exposure becomes more difficult and time consuming. We present a heuristic approach where the mechanical and thermal aspects of devices are exploited to quickly identify MVRs. Our approach involves the topological mapping of two device conditions. The first condition identifies regions with the highest mechanical strain or density of defects and interfaces via thermal wave probing and phase analysis. The second condition identifies regions with high electrical field. It is hypothesized that the region with the highest thermal wave penetration resistance and electrical field will exhibit the highest sensitivity to incoming radiation for single events and potentially, total ionizing dose. Our approach implements a simplistic design that improves analysis time by ∼2–3 orders of magnitude over current radiation sensitivity mapping methods. The design is demonstrated on the well-studied operational amplifier LM124, which shows agreement with the literature in identifying sensitive transistors–QR1, Q9, and Q18–with relatively high phase percentile values (>70%) and ΔT percentiles (>50%), satisfying conditions for elevated radiation susceptibility. This is followed by experimental results on a static random access memory (HM-6504) and a Xilinx Artix-7 35 T system on a chip.
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The importance of identifying radiation sensitive regions within electronic systems is ever increasing as many crucial electronic devices operate in damaging radiation environments, such as space, aviation, defense, medicine, and nuclear power. Radiation induced upsets and damage pose a significant threat to the reliability of such electronics, producing large amounts of ionization and inducing charge carrier traps which result in system failures ranging from temporary loss of data to the complete and permanent loss of functionality.[1] To remedy this, reducing the susceptibility of electronic systems, such as microprocessors or memories must begin by identifying the most vulnerable regions (MVR) to ionizing radiation, after which efforts to improve their radiation hardness may be undertaken. The complexity of this task is increasing, commensurate to that of the increasing integration levels and component density of electronic systems. For example, the evolution of the system-on-a-chip (SOC) has seen intricate architecture with complex chains of operation, from which it is very difficult to pinpoint the MVR based on a global circuit response to incoming ionizing radiation.[2] Therefore, even though the state of the art in the identification of radiation damage of electronics has developed significant insights at the component level, identifying the vulnerability of the SOC remains as challenging as ever.[3,4]

Ionizing radiation takes the form of either atomic particles or electromagnetic waves, which have sufficient energy to strip a localized electron from atoms in the target and lead to energy deposition in the form of ionization or displaced atoms. Ionizing radiation has two main categorized effects on electronics, the first of which is total ionizing dose (TID), normally detectable as near-surface damage. In this case, changes are manifested mainly in oxide layers that are present in field effect transistor (FET) and bipolar junction transistor (BJT) devices due to the net positive charge and charge traps left at the oxide interfaces after electrons are carried away by existing electric fields.[5,6] The second main effect of ionizing radiation on electronics is caused by single event effects (SEE), in which a single incoming ion interaction causes a large, detectable ionization due to a current transient.[7,8] In both cases, charge traps are created, reducing the mobility of charge carriers and increasing the leakage current and threshold voltage, resulting in device faults[9–11] The charge production and diffusion following interaction of target atoms with energetic radiation are probabilistic, because several variables, such as the incoming energy, angle of incidence, and material properties, will define the degree of ionization. At the same time, the location of the track (with respect to charge collectors, such as the drain) as well as the local dynamics of the circuit govern how damaging such an ionizing track is at the system level. Across a chip, the variation in composition, device structure, and charge density will affect the level of sensitivity to incoming radiation, and certain regions will be particularly sensitive to radiation based on these factors. Identifying these sensitive regions are of high importance for improving the radiation hardness of devices.

Current approaches for detecting radiation sensitivity in electronic systems are limited by time and cost. The direct approach involves the detection of errors during or after exposure to ionizing radiation. There are difficulties associated with the design and control of such an experiment, where collimation and masking are often required for isolation of a single system component, especially when considering complex SOCs. These experiments are also often costly due to the limited number of facilities that have the capability to expose devices to gamma rays, ions, neutrons, protons, etc Perhaps the biggest challenge is to extract an error signal from the system level and even more so to pin-point the upset location[12] This is particularly true for studies employing broad-beam ionizing radiation sources. The use of field programmable gate arrays (FPGA) have been particularly effective in many cases due to the versatility of their programming and uniformity of gates.[13] Similarly, significant efforts have been undertaken with micro-beams, which mitigates the challenge of the spatial precision of detection at the expense of experimental setup complexity.[4] A very effective version of this approach uses a pulsed laser source as a surrogate for ionizing radiation to inject carriers at a known location. For this technique, a micron-sized, pulsed laser deposits charge

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while scanning across a device to map regions that generate the largest transient pulses, which indicate radiation sensitivity[14–17] However, analysis is time-prohibitive because mapping must be done at various energy levels to quantify the linear energy transfer (LET) for each position and the device must be allowed to fully relax to its equilibrium state between each laser pulse.[4] Collecting high spatial resolution measurements does not pose a problem for pulsed laser scanning, but doing so while registering the transient currents consumes significant time. The technique is thus typically applied to a length scale of several tens of microns, while system level devices span millimeters in length.

In general, existing electrical domain techniques, where a critical charge is generated to cause a detectable error, inherently require lengthy analysis to identify regions that are particularly sensitive to radiation damage.[4] Alternate methods to examine radiation sensitivity of electronic systems, which reduce time and cost associated with analysis, would be attractive for high throughput analysis of entire devices. An additional approach utilizes software-based methods for diagnosing errors in devices in radiation environments. Here, faults are artificially injected to the system while studying the output to achieve a deep insight to the global circuit response to local faults. However, this approach requires an intimate understanding of the device being interrogated as well as a modeling framework that can facilitate the identification of faults and system failures in a complex SOC.

Proposed Heuristic Approach

From a fundamental perspective, locating the MVR in an electronic chip is to some degree, analogous to locating the regions with the highest electrical field. This is because only an electrical "hotspot," as shown in Fig. 1a, can allow enough diffusion of current to cause an upset from the transient. However, mapping electrical field is not sufficient to detect MVRs, or else the problem would essentially reduce to simulation mapping for field strength. Following the same logic, it would predict uniform radiation sensitivity in a uniform architecture chip (such as an array of SRAM cells), which does not occur in reality.[18] It would also not explain multiple bit upset events. Rather, the literature shows inherent stochasticity in SEE in electronics that cannot be deciphered by investigating the electrical field alone. This is exacerbated by the sheer number of variables related to incoming radiation; device size, type, and materials as well as characteristic strength and drawbacks of characterization methodologies.

In this study, we propose that SEE phenomena are influenced by a mechanical field (in addition to the electrical field typically considered), which may exhibit high stress regions or "mechanical hotspots." The concept is motivated by the fact that existing approaches consider the electrical domain only, thereby overlooking the non-idealities in materials and fabrication issues. Real systems routinely experience departure from ideal conditions as well as mechanical stress build-up in the system due to the lattice and thermal expansion mismatch in the various film layers and the substrate. These interfacial stresses conglomerate into complex 3-dimensional states at the device's out-of-plane features (e.g. gates or vias). Stress concentrations continually increase the field in a localized manner so that shrinking device size implies possibly higher stress states. Such localized states most commonly coincide with the edges of device features, such as the gate, and attenuate vary rapidly. Even though the average stress value may not appear to be significant, the localized values can reach up to a few GPa.[19] Such high mechanical stress implies that the atoms are already far from equilibrium positions and may require less energy to become ionized compared to the unstressed material. We therefore propose that the mechanical hotspots—introduced due to materials and fabrication deviations and exacerbated by device scaling—can play a significant role in ionization events. At the same time, the electrical field plays a significant role in the buildup and transfer of the critical charge to actually disrupt the electrical state or behavior of the system. Such effect of localized stress is schematically shown in Fig. 1b, where the funnel representing charge drift is locally distorted since the amount of charge generated is increased by the stress. This is in addition to the mechanical stress concentrations at the gate/drain edges, which are inherently present from processing and could play a pivotal role in SEE phenomena.[20] Investigating stress localization in electronic devices can therefore potentially explain their radiation sensitivity. Unfortunately, only a few studies into these effects exist in the literature, but they consistently show the deleterious effects of mechanical stress/strain on radiation vulnerability.[14,21]

However, mapping strain hotspots over a large area is not an easy task, as most techniques that are well suited for strain measurements either probe lattice strain at the nanoscale or over a large, averaged area. We explore thermal wave probing as a means for indirectly mapping strain that is caused by device layering and interfaces. Even though the dynamics of an energetic particle and a phonon wave are not the same, we propose strained lattices and interfaces will provide relatively higher resistance to both compared to a relaxed device. Results from the literature show that charge collection in silicon-on-insulator (SOI) devices possess a remarkable dependence on strain, where an increased number of charge traps are filled in strained devices.[21] Because fewer charge traps will affect the mobility of charge carrier in strained devices, more charge carriers are able to deposit and cause an upset after an ionization event, which essentially increases the stopping power. However, more factors must be considered to identify the most sensitive regions on a chip; identifying regions that offer the highest stopping power of radiation is only the first step. The second step is to ascertain that the same region is also electrically relevant, meaning that there is also a high electric field, electron mobility, and a drain or a terminal to deposit the generated charge.

We propose a two-pronged approach for identifying radiation sensitive components: (a) the first utilizes lock-in thermography (LIT) to map areas of high radiation stopping power, where thermal waves are uniformly injected without electrical biasing to probe the

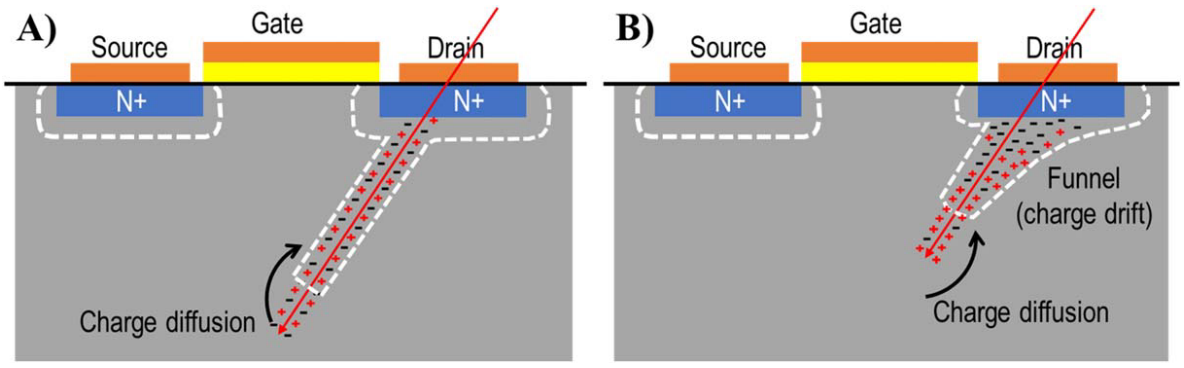

Figure 1. Schematic of charge carrier generation and collection (a) during and (b) immediately following an energetic particle striking a node in a field effect transistor (FET), where the white dashed lines indicate the evolution of the depletion region following a single event, resulting in a transient current at the node.

subsurface features of a standard operational amplifier (LM124). (b) The second utilizes electrical biasing of the same LM124 system to identify regions that exhibit high electric activity. This is done by measuring the increased thermal output response after powering. LIT is ideal for probing the subsurface features of the LM124 because it is a non-contact, non-destructive technique with high temperature sensitivity, capable of detecting and mapping surface and subsurface inhomogeneities that interrupt thermal wave propagation through a material. This technique has been used as a nondestructive method for detecting defective components in integrated circuits[22–26] Several application fields of lock-in thermography—especially for analytical diagnoses and mapping of faults in microelectronic devices—have been evaluated by Breitenstein.[22] The lock-in detection strategy relies upon periodic injection of heat into a device with concurrent temperature measurement via an infrared camera to analyze the reemitted infrared signal. This method takes merely hours to measure an entire chip as opposed the months or years that it would take existing high spatial resolution techniques to measure the same chip.[4] These techniques use a tightly focused laser to imitate the effects of ionizing radiation and thus do not have a coarse resolution embodiment. In comparison, the proposed technique is fundamentally different from the existing literature. There is no need to imitate the ionizing radiation. Rather, we detect regions of localized stress/strain on the large chip. This is then used to validate a hypothesis that strained regions are easier to ionize compared relaxed regions.

LIT phase contrast analysis was explored to identify regions that exhibit the highest altered thermal wave propagation, where increased phase lag indicates regions that would experience high energy deposition during irradiation of the entire device.[22,27,28] Additionally, no contrast in the phase map is a result of local IR emissivity differences across the surface of analyzed devices because they are computed from a ratio of the S^{90° and the S^{0° signal, which are each accurately proportional to local emissivity. Therefore phase maps are uniquely beneficial for examining inhomogeneous surfaces like those of integrated circuits, which feature a range of materials with large differences in emissivity.[22] For this work, analysis of devices via lock-in thermography and electric field mapping can identify regions that are most sensitive to radiation induced damage or upsets, which result in defective device performance.

Experimental Methods

Testing was carried out on the operational amplifier LM124, which represents a standard component. The device was delidded to expose the components for thermal analysis. Figure 2 shows an optical micrograph of one quadrant of the de-lidded operational amplifier.

- Lock-in Thermography Measurement: In this work, an Optris PI 640 IR camera with a nominal thermal sensitivity (i.e. noise equivalent temperature difference) of 75 mK over the spectral range of 8–14 μm was utilized. Each video frame contains 640 × 480 pixels of temperature data, and 2000 frames of data were processed for each measurement. Due to the time-averaging nature of LIT, up to two orders of magnitude improvement in the thermal sensitivity was possible, allowing the discernment of slight differences in subsurface inhomogeneities after digital lock-in signal processing from stored thermal datasets.[22] The lock-in thermography setup is composed of three components, including an infrared (IR) camera, a thermal excitation source, and a signal processing tool as schematically drawn in Fig. 3. An IR microscopic lens with a focal distance of 41.5 mm and a resolution of 28 μm was used. All measurements were acquired at a frame rate of 32 Hz, which is the standard framerate of the PI 640 camera. This framerate enables enough volume of data per lock-in period for accurate analysis. Note that thermal cameras with special resolution limits of less than 5 μm exist, which could benefit this technique for future studies.[29] Two heat lamps were pulsed using a two-channel 5 V relay module and a programmable Arduino board. The relay acted as a switch for the lamps that were powered by a 120 V/60 Hz wall outlet. Measurements were collected after the boards were exposed to the pulsing heat lamps for 30 minutes, which was sufficient time to reach and maintain a consistent average temperature throughout the entirety of the measurement.
- Field Measurements: Relative electric field measurements on the operational amplifier LM124 were obtained by measuring the temperature change following the powering of the device in an inverting amplifier configuration with an input voltage of 0.5 V, a voltage gain of 2.75, and a power supply of ±10 V. The thermal measurements were measured with the Optris PI 640 infrared camera.
- Signal Processing: All thermal signal processing was conducted post measurement in Matlab R2020a. The lock-in correlation procedure requires the removal of noise from the signal by filtering signal that does not modulate at the lock-in frequency. Noise present in the raw thermal signal was removed using a forward and reverse band pass filtering sequence to ensure zero phase distortion of the raw data. Figure 4 shows the result of the filtering process for the time-dependent temperature, where the majority of the noise is subtracted from the raw signal, resulting in a nearly harmonic filtered signal.

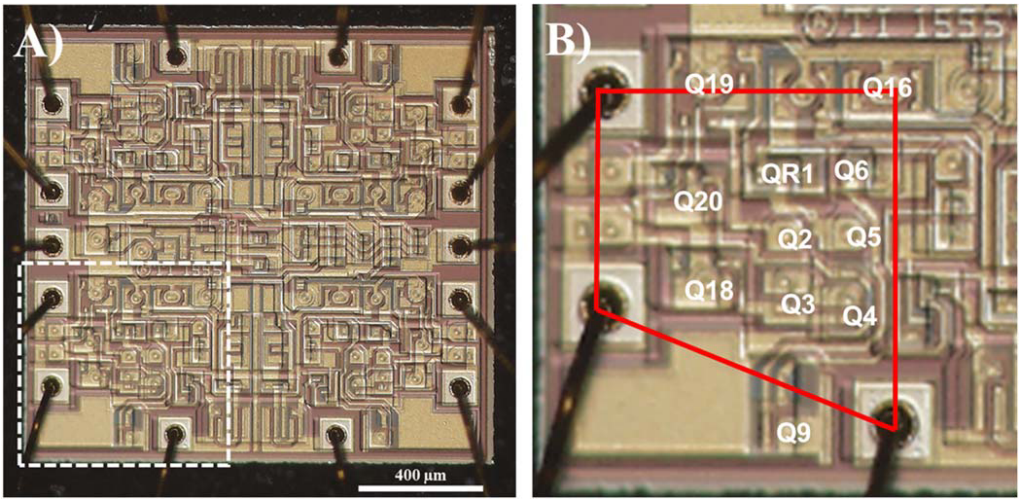

Figure 2. Optical micrograph of delidded operational amplifier LM124.

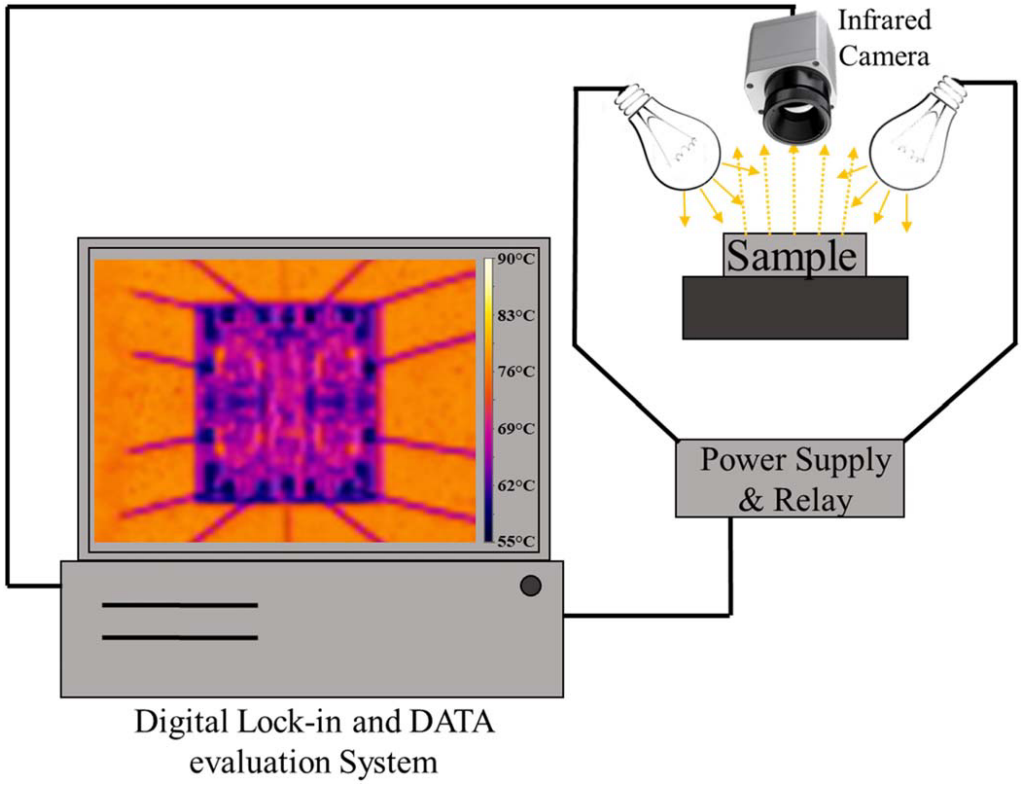

Figure 3. Schematic of illuminated Lock-in Thermography (ILIT) Setup.

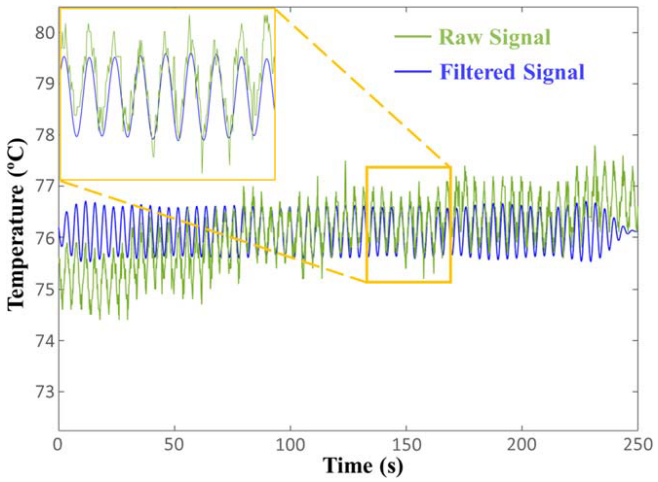

Figure 4. Comparison of raw thermal input for a single pixel and filtered thermal signal for continued processing.

•Lock-in analysis of thermal video files were conducted by weighting the reemitted thermal signal with two sets of orthogonal weighting factors (i.e. sin(t) and -cos(t)) as a function of time and summing the results for each pixel in a frame storage. After summation, each pixel contains two signal values, including (1) S^{0°, which is the in-phase component of the reemitted signal and (2) S^{-90°, which is the out of phase component of the reemitted signal.[22] Both the S^{0° and S^{90° signals are used to calculate the phase value for each pixel according to Eq. 1, where the phase value represents the amount of lag of reemitted thermal signal relative to a reference signal.

$$Phase = \tan^{-1}(S^{-90^\circ}/S^{0^\circ}) \quad [1]$$

Higher phase contrast values indicate regions with higher thermal stopping power due to the underlying structure of the device and present strain fields. It is important to note that there are no contributions from local emissivity variation on the surface of integrated circuits to the contrast of the phase map. This is because the phase value is calculated from the ratio of the two thermal datasets, S^{0° and S^{-90°, which are each individually proportional to local emissivity.[22]

Results

Lock-in analysis was conducted on the entire face of the operational amplifier LM124 and a phase map was constructed from the results. The measurement was collected over a 250 second period where the LM124 was thermally pulsed with thermal lamps at a frequency of 0.25 Hz, which was chosen to ensure sufficient sampling for each lock-in period given that heat is introduced non-harmonically.[22] Additionally, phase contrast was at an apparent local maximum usinga lock-in frequency of 0.25 Hz, which provided the highest signal-to-noise ratio for analyzing results. Figure 5 shows the optical micrograph and LIT phase map of the entire LM124, including labels for the most sensitive transistors–identified with a "Q" to denote a transistor–to single event transients (SET), which are Q2–6, Q9, Q16, Q18–20 and QR1.[30] Transistor QR1 has a slight exception to its nomenclature because it has been identified by most authors that are concerned with the LM124 as having a transistor structure whereas the manufacturer denotes it with an "R1"[31–33] Note that the phase map is emissivity corrected, and any contrast in the phase response is due to the interaction of the thermal waves within the LM124 with surface and subsurface strain and features. From the phase map it is apparent that certain transistors on the LM124 are highlighted as having high phase contrast, indicating mechanical susceptibility. However, according to our proposed reasoning, the electrical hotspots must be identified as well to distinguish radiation sensitive regions.

Identifying regions with high electrical activity is a more challenging task, which we have simplified by suggesting that

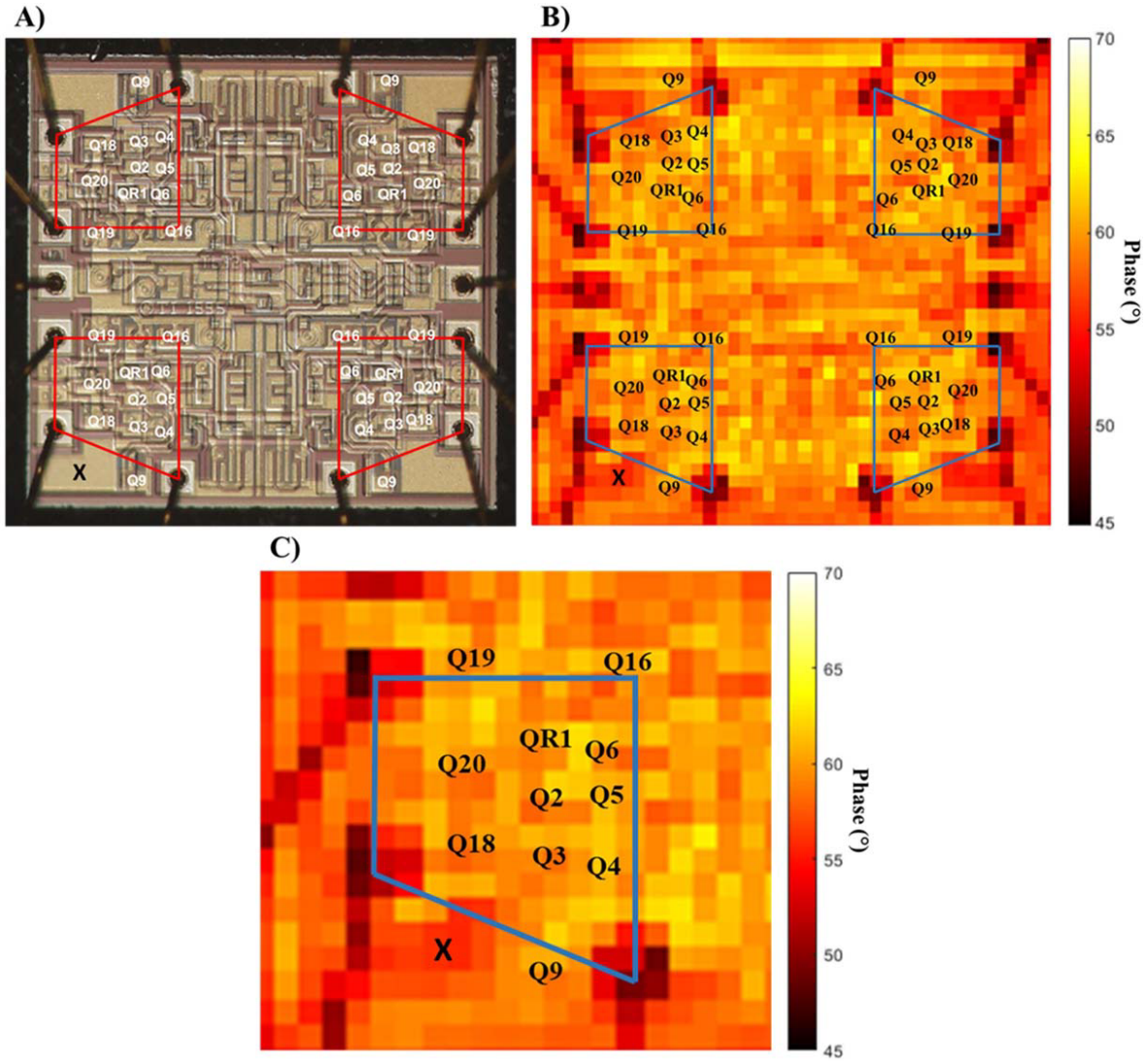

Figure 5. (a) Optical micrograph of the operational amplifier LM124, (b) lock-in thermography phase map with labelled transistors, and (c) enhanced magnification of bottom left quadrant of the phase map.

regions with high electrical activity show a greater increase in the temperature. Thermal images were captured of the LM124 in both a powered and unpowered state to identify regions that exhibit the highest electrical activity. While thermal identification of electrical hotspots may not necessarily universally hold, we note that thermal hotspots generally indicate electrical hotspots. Figure 6 shows the contrast prior to and after powering.

Together, the phase and thermal maps in Figs. 5 and 6 are compared to identify the regions that satisfied both mechanical and electrical conditions for MVRs. As a comparison, a capacitive pad that is labelled with an "X" in Fig. 6, which is known to be less susceptible to radiation effects has been included in the numerical analysis. Table I shows the average phase and changes in temperature (ΔT) values for a representative set of transistors and board components. These values are reported as percentiles for the entire board, where higher percentiles indicate a relatively high value for the entire LM124. Higher values of phase difference indicate mechanical hotspots, while higher values of ΔT indicate high electrical hotspots due to Joule heating after powering. If a region on the board indicates relatively high phase and ΔT values, both conditions of an MVR are satisfied, and it is flagged as sensitive to radiation damage. Our results show that the QR1 transistor has the highest product of phase and temperature differences, making it the most SEE sensitive region in the entire LM124 chip. This finding agrees with all similar studies on LM124 reported in the literature. We also identify other significant regions; the Q9 and Q18 transistors. The LM124 is well studied in the literature and the results from previous finding performed with a pulsed laser are very consistent with our findings.[4,31–37]

Discussion

Existing radiation sensitivity measurement techniques predominantly depend on electrical response of devices or circuits. Little or no consideration is given on materials or processing aspects of a system. Or in other words, effects of stress localization arising from lattice mismatch, processing conditions, or fabrication errors are not explicitly considered. The essence of our new heuristic approach takes the form of a composite metric; where radiation sensitivity is a product of the electrical (for example gate area in a transistor) and materials (for example stress concentration areas) sensitivity. The implication is that if we consider a uniform array of devices, conventional approaches will predict uniform SEE sensitivity, whereas our approach will predict the particular devices with localized built-in stress as sensitive ones. To highlight this, we note that there are some locations in the Op-amp LM124 which are highlighted as either strong mechanical or electrical hotspots, but not both. For example, the capacitor located at position "X" (in Fig. 5) exhibits high electrical activity from the increase in thermal signal,

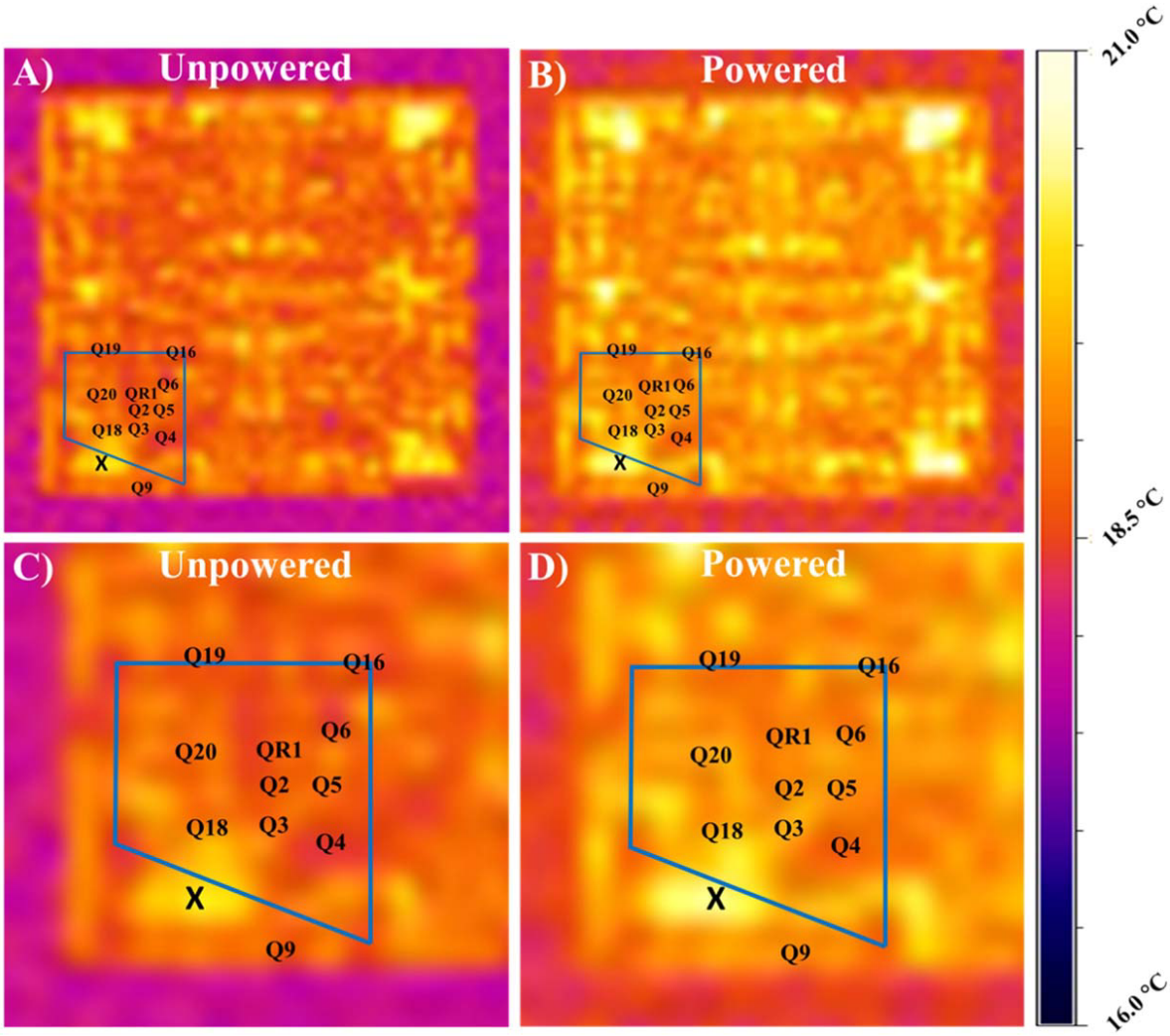

Figure 6. Thermal micrograph of the operational amplifier LM124 (a) at a uniform room temperature and (b) after powering, and the accompanying enhanced magnification of the lower left quadrant (c)–(d).

Table I. Phase and temperature values of LM124 transistors.

Transistor	QR1	Q9	Q18	Q20	"X"
Phase Percentile	85.1	76.3	71.5	69.6	54.6
ΔT Percentile	60.0	60.0	58.3	51.7	68.3

but not mechanical susceptibility according to the phase map. Because only one of the two conditions are met, the capacitive pad would not be highlighted as an MVR. It is known that the capacitors are not as susceptible to upsets from irradiation as features, such as transistors.[36,38]

In addition to the results from the operational amplifier LM124, preliminary lock-in phase analysis was conducted on a Xilinx Arty A7 FPGA and an SRAM HM6504 as seen in Figs. 7 and 8, respectively. From the phase map of the FPGA, it is apparent that certain structures on the board show a high phase contrast relative to the rest of the board, such as the configurable logic blocks and the input/output pads, indicating an increased stopping power for ionizing radiation. However, the electrical relevance of each of these structures is also necessary to determine their overall vulnerability to ionizing radiation.

The features in the SRAM in Fig. 8b are less distinguishable by phase analysis compared to the FPGA in Fig. 7b because the feature sizes are considerably smaller and are uniform in geometry and spacial distribution at the limit of diffraction of the infrared light used to make the measurement. However, an apparent shift in the phase contrast from the upper half of the phase map to the lower half may indicate a distribution in strain across the device as a result of the manufacturing process, which indicates that the structures in the upper region may be more susceptible to SEE events. Note that surface contaminants remaining on the device after the delidding process are visible in the optical micrograph and account for the darkest region on the SRAM phase map and do not indicate the response of the device alone.

The advantage of the proposed MVR detection technique is that it heuristically determines the likely SEE sensitivity, without the actual need for radiation experiments. It also significantly reduces the amount of analysis time and is particularly suitable for large array of identical devices (such as logic gates). However, the heuristic nature of the proposed technique warrants more work for validation. It is true that a plethora of SEE-related works exist in the literature. However, all these involve circuit response to energetic particles, whereas our proposed technique does not need any data on circuits. Therefore, validation of the technique requires comparable mapping of the sensitive areas on the device real estate. For example, Figs. 7 and 8 maps the SEE sensitive areas, for which no other comparable sensitive region mapping exists in the literature. Currently, we are considering employing the pulsed laser technique for such validation, which is also challenging for time and other resources,

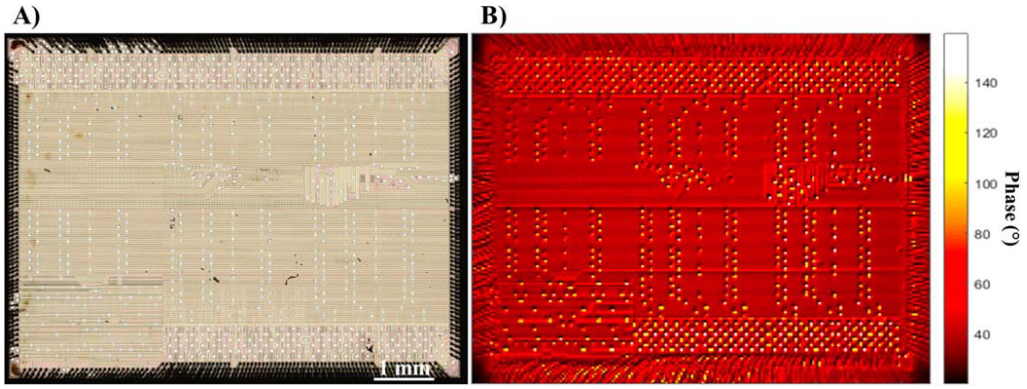

Figure 7. (a) Optical micrograph and (b) lock-in thermography phase map of Xilinx Arty A7 FPGA.

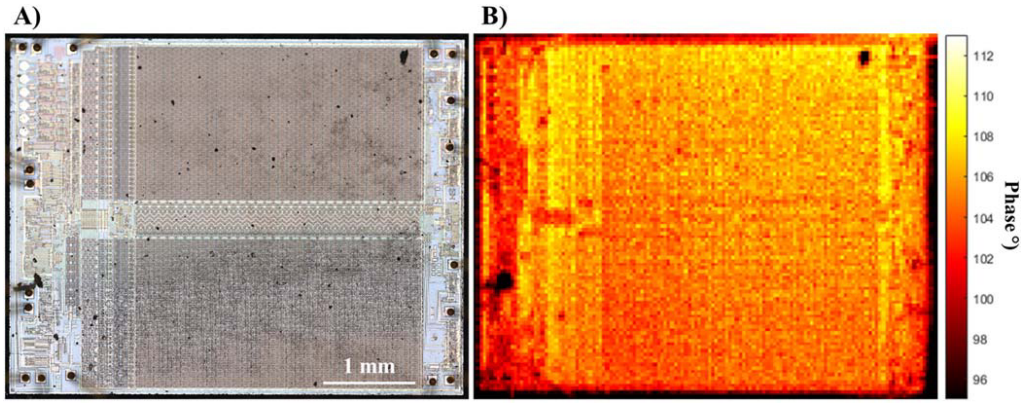

Figure 8. (a) Optical micrograph and (b) lock-in thermography phase map of SRAM HM6504.

considering the large area of the modern SoCs. Additionally, this technique is inherently limited in spatial resolution due to the diffraction limit of the infrared light used to probe the electronics. Though this technique could not be used for pinpointing the locations to sub-micron accuracy, it harbors great potential to reduce the time it takes to analyze a large, complex devices by providing a methodology to identify most vulnerable regions very quickly. Subsequent analysis by better spacially resolved techniques, such as single event transient testing with a pulsed-laser, could then better examine the regions highlighted by phase and electrical domain analysis.

Conclusions

This study presents a novel heuristic technique for quick identification of radiation sensitive regions on large area and complex SoCs. Here, localized mechanical stress is hypothesized to influence SEE sensitivity, in tandem with electrical field. The proposed technique is demonstrated on an operation amplifier LM124 for which SEE sensitive region mapping is already available in the literature. In addition, the technique was applied on a RAM and FPGA. The mechanical hot spots within the devices were mapped using pulsed thermal phase analysis via lock-in thermography. Regions with high phase contrast were compared to regions that exhibit elevated electrical activity when the LM124 is powered. When both conditions are met for the same region, that region was identified as vulnerable to radiation induced upsets.

The results from this study identified transistors QR1, Q9, and Q18 on the LM124 as the most vulnerable regions to radiation induced upsets, at relatively high phase percentiles of 85.1, 76.3, and 71.5, and ΔT percentiles of 60.0, 60.0, and 58.3, respectively. Whereas a region known to be less sensitive to radiation effects had fairly average phase and ΔT percentile values at 54.6 and 68.3, respectively. These results are consistent with previous studies on the LM124 using pulsed laser techniques. This serves as a reasonable validation for our new philosophy, where no ionization event is required to accurately identify MVRs. Future work can significantly reduce time required for analysis of electronics, especially for larger and more complex devices, for which traditional analysis would take 2–3 orders of magnitude more time to complete.

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