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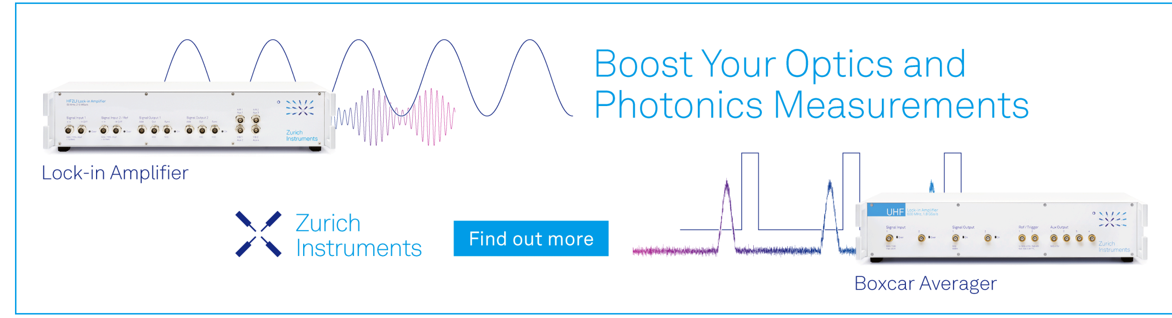

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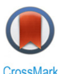
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ABSTRACT

In this work, we demonstrate the rejuvenation of Ti/4H-SiC Schottky barrier diodes after forward current-induced degradation, at room temperature and in a few seconds, by exploiting the physics of high-energy electron interactions with defects. The diodes were intentionally degraded to a 42% decrease in forward current and a 9% increase in leakage current through accelerated electrical stressing. The key feature of our proposed rejuvenation process is very high current density electrical pulsing with low frequency and duty cycle to suppress any temperature rise. The primary stimulus is, therefore, the electron wind force, which is derived from the loss of the momentum of the high energy electrons upon collision with the defects. Such defect-specific or "just in location" mobilization of atoms allows a significant decrease in defect concentration, which is not possible with conventional thermal annealing that requires higher temperatures and longer times. We show evidence of rejuvenation with additional improvement in leakage current (16%) and forward current (38%) beyond the pristine condition. Transmission electron microscopy, geometric phase analysis, Raman spectroscopy, and energy dispersive x-ray-spectroscopy reveal the enhancement of defects and interfaces. The ultrafast and room temperature process has the potential for rejuvenating electronic devices operating in high power and harsh environmental conditions.

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SiC Schottky diodes are attractive for harsh environment applications, including high-performance ultraviolet (UV) photodetectors in high-temperature environments, power factor correction in high-end AC/DC power supplies, high-frequency power supplies, power factor correction, power conversion in motor controls or power management appliances, reverse polarity protection, etc.[1,2] Furthermore, SiC detectors have the potential to be used in x-ray imaging systems and EUV (extreme ultraviolet) detection for astronomy radiation imaging due to their radiation hardness feature.[3–5] 4H-SiC is one of the polymorphs of SiC with a large bandgap (3.3 eV), the highest critical electric field, high saturation velocity of electrons, and high thermal conductivity.[6] These properties are often deteriorated by various kinds of defects and traps,[7–9] causing non-uniformities in electrical behavior, reduction in breakdown voltage, increase in leakage current and noise, and even complete failure.[10,11] Various methods have been reported in the literature for defects mitigation, such as temperature control in sublimation-grown SiC bulk crystals to reduce thermal stresses,[12] optimization of growth methods and process parameters,[11,13] thermal oxidation/thermal annealing or C ion implantation/thermal annealing,[14] and *in situ* pre-growth etch before growth.[15]

In this study, we present an approach to mitigate defects in electronic devices without raising the temperature. The basic process involves passing high density current pulses through the specimen. Inside the lattice, the electron scattering produces Joule heating. At the same time, whenever scattered by defects, the electrons lose their momentum. Such momentum transfer imparts a mechanical force to defective atoms.[16] This is known as the electron wind force (EWF) in classical electromigration (a damage phenomenon) literature.[17] In electromigration, Joule heating creates thermomechanical stresses, introducing defects. The temperature-defect growth process is

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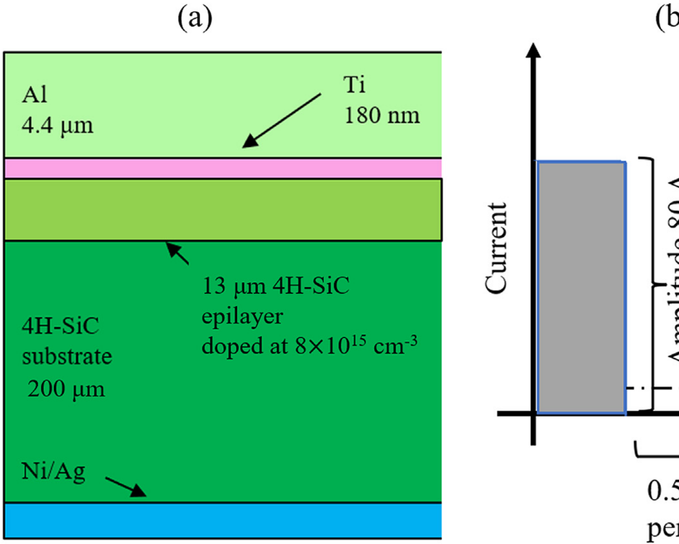
self-compounding, meaning that the defects increase the Joule heating, which in turn increases defect size and/or density—culminating in an uncontrollable temperature rise. The thermal domain overshadows the EWF, which produces convection–diffusion of solid atoms to cause growth of hillock and void features. In our process, the distinctive departure to this well-known damage phenomenon is our suppression of thermal domain. We achieve this by using low frequency and low duty cycle current pulses. The sharp current pulses in this study may generate thermal spikes, but the overall temperature is maintained at ambient. This allows the EWF to be the predominant force in the process. Since the EWF is generated only on defective atoms, the unique specificity implies a faster and energy efficient pathway toward lower defect concentration and higher electron mobility. In comparison, conventional thermal annealing involves uniform heating of both crystalline lattice and defective atoms. More details are presented in the later paragraphs.

The above-mentioned EWF-based approach has been proved effective in 2D materials,[18,19] metallic thin films,[20] and GaN HEMT devices.[21] Foundational aspect of the EWF approach is given in the literature,[22,23] which also reports enhanced plasticity in materials that are typically very hard and brittle. There are a few potential explanations, including thermal effects from Joule heating,[24] electron winds,[25,26] and electrostatic fields.[27] Kim *et al.* established in their studies that annealing may be induced by an electric current in a manner distinct from Joule heating in an aluminum alloy.[28] It is well established that the application of pulsed electric current in metals or alloys promotes the coalescence of sub-grains, accelerates recrystallization, and creates new, strain-free grains, which manifest the athermal effect of electromigration or EWF.[29–32]

Commercially available (GP3D030A120X, SemiQ) 30 A 1200 V Schottky Barrier Diode (SBD) based on 4H, N-type SiC were used in this study. The die size is $2.16 \times 2.16\,\text{mm}^2$, with Al/Ti metallization as an anode and Ni/Ag as a cathode. This is shown in Fig. 1(a). This diode is made of a first thin 180 nm Ti metal layer to form the Schottky contact on the semiconductor surface. On top of this contact metallization, a thick layer (4.4 μm) of Al is deposited to reduce the thin contact metal's parasitic resistance (Ti) and increase the diode current capability. For electro pulsing, a DC power supply (Sorensen DCS100-12E) is used with a current pulse generator (Laser Controller, ED2P-AXA-0032) to apply up to 80 A current. To minimize the temperature, we used 20 μs pulses at 2 Hz frequency as depicted in Fig. 1(b). The experiments are carried out under an Optris PI 640 thermal microscope to track the die temperature in real-time. For the microanalysis, electron transparent samples from the die are prepared in Scios 2 DualBeam with Ga ion focused ion beam (FIB). We performed transmission electron microscope (TEM) imaging and energy dispersive x-ray analysis in a 200 kV FEI Talos F200X S/TEM with 1.2 Å resolution.

To demonstrate the effectiveness of EWF-based rejuvenation, we first intentionally degrade the SiC SBDs. Accelerated degradation was carried out by electrically stressing the devices at the forward current density of 25 A/cm^2. For an unpackaged device, with no thermal management, this current density appeared to degrade forward current by about 50%. Post-stressing characterization was performed after 48 h to check for any time dependent recovery. We measure a post-stressing increase in leakage current by up to 9%, a 42% decrease in forward current, and a reduction of barrier height by 12% as shown in Figs. 2(a), 2(b), and 3(a), respectively. Defects, such as vacancies, interstitial, or dislocation, have their energy levels deep inside the bandgap of the semiconductor. These deep-level defects will serve as free-charge carrier trapping centers and lower their concentration in the material. Furthermore, the defects that are produced will serve as scattering centers, reducing the mobility of charge carriers. Due to the inverse relationship between series resistance and mobility and carrier concentration, the devices' series resistance would rise because of the drop in mobility and carrier concentration in both the epilayer and substrate.

The generation of defects near Ti and 4H-SiC contacts after stressing can cause both increase in leakage current and a decrease in the Schottky barrier height.[33] The decrease in forward current may arise from the increased resistance in the bulk SiC due to defects



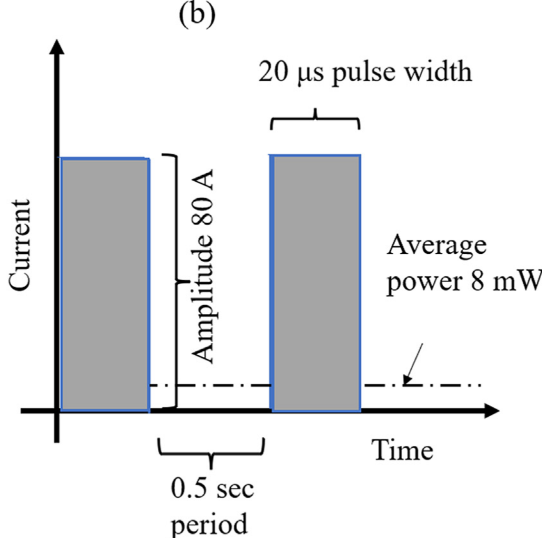


FIG. 1. (a) Schematic of the cross section of the SiC diode sample. (b) Low duty cycle current pulsing scheme for EWF-based ultrafast, room temperature rejuvenation.

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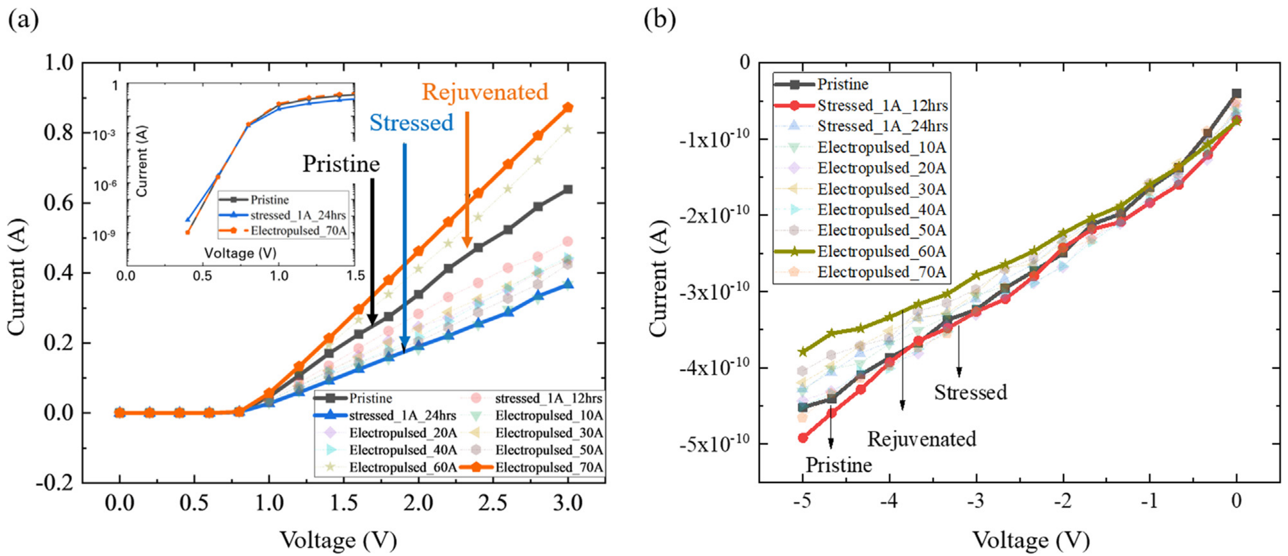

FIG. 2. Effect of electrical stressing and electro pulsing on (a) forward and (b) reverse voltage I–V curve. Thicker linewidths indicate the pristine, degraded, and rejuvenated phases. The inset of (a) shows the semi-log plot of the forward I–V curve. Post-rejuvenation characterization was performed 48 h after the processing to avoid any short term effect.

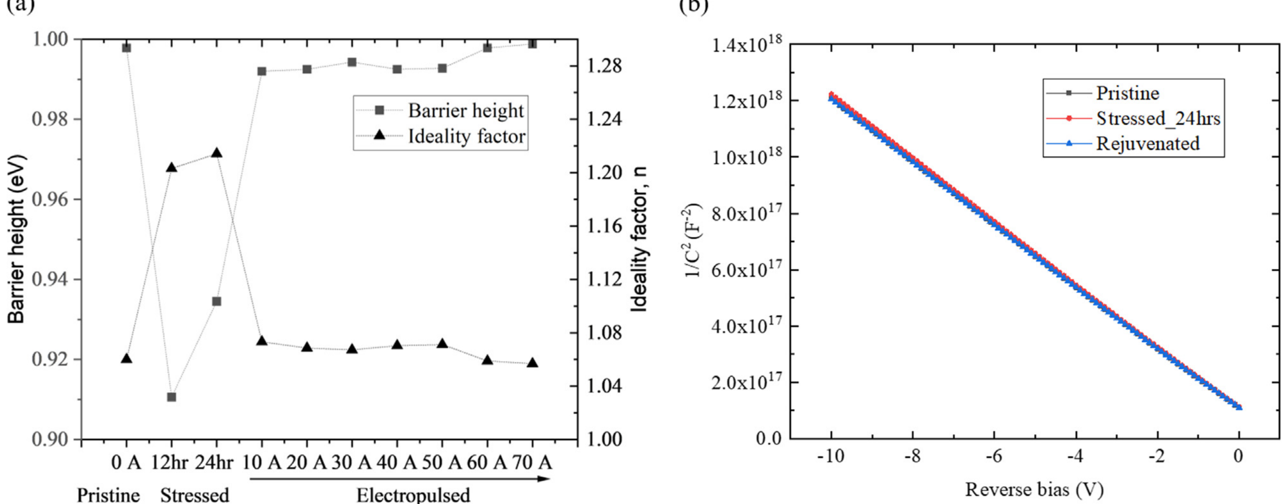

FIG. 3. (a) Change in barrier height and ideality factor after electrical stressing and electro pulsing. (b) $1/C^2$ vs V characteristics.

generated from a high electrical field. Here, thermionic emission model is used for forward current density, which is given by

$$J = J_s \exp\left(\frac{qV}{nkT} - 1\right) = A^{**}T^2 \exp\left(-\frac{q\emptyset_{bn}}{kT}\right)\exp\left(\frac{qV}{nkT} - 1\right).$$

Here, J_s is saturation current density, J is current density, A^{**} is Richardson constant for the metal/semiconductor interface, and $\emptyset_{bn}$ is Schottky barrier height. Taking log on both sides and plotting a semi-log J–V curve, which should be linear for thermionic emission and can be used to extract the barrier height, ideality factor, and saturation current density. The y-intercept of the J–V curve gives the value of the saturation current density, J_s from which $\emptyset_{bn}$ is calculated $[\emptyset_{bn} = \frac{kT}{q}\ln(\frac{A^{**}T^2}{J_s})]$, and the ideality factor, n, can be extracted from the slope using the equation $n = \frac{q}{kT}(\frac{dV}{d\ln J})$. The ideality factor, n, is a parameter that describes the deviation of a diode's behavior from ideal diode characteristics. It provides information about the electron transport mechanism involved in the Schottky junction. An ideality factor close to unity means that all the current is generated by thermionic emission. Values above unity reveal other electron transport mechanisms, like trapping or tunneling, carrier recombination at surface states near the metal–semiconductor interface, and diffusion of electrons or holes.

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The degraded devices were then rejuvenated with 4% duty cycle pulses of (20 μs electrical pulses at 2 Hz frequency) high current (up to 80 A) passed through the diode for about 30 s. Most of the rejuvenation that takes place in the first few seconds. Figure 2 shows the experimental results where the three distinct stages (pristine, stressed, and rejuvenated) are marked with thicker linewidth for visual guidance. Figure 2 also shows the effects of the various magnitudes of pulsed currents. At 40 A current pulses, the leakage current is fully recovered. Intriguingly, a further 16% reduction in leakage current than pristine devices is achieved after 60 A current pulsing as shown in Fig. 2(b). The relatively low leakage current of the electrically annealed device is the result of decrease in defects (structural defects, point defects, and impurities), which are generated near the semiconductor surface when the metal contact is deposited on this surface. These defects produce a large density of surface states defects in the forbidden gap of a semiconductor, which enables flow of leakage current through the depletion layer. We obtained not only full recovery of the devices but also 38% increase in forward current compared to the pristine condition after applying 70 A pulses shown in Fig. 2(a). In addition, from the inset, Fig. 2(a) shows that stressed devices exhibit larger subthreshold swing than pristine and rejuvenated devices. The Ti metal contact in the SiC Schottky diode in our investigation may underwent a similar improvement (shown later by electron diffraction technique). The dislocation defects induced in SiC from electrical stressing scatter electron and generate EWF, which can improve dislocation mobility by lowering activation energy of dislocation.[34]

Electrical stress can increase Schottky barrier height through the introduction of impurities or defects, such as dislocations, vacancies, or interstitials, altering the interface properties. Electrical stress can also lead to the creation of surface states at the metal–semiconductor interface. Surface states can trap charge carriers, leading to an increase in the effective barrier height.[35] After rejuvenation, the barrier height and ideality factor returned close to their original values as shown in Fig. 3(a). C–V measurements plotted as $1/C^2$ vs V_R should yield a straight line with a slope of $2/q\varepsilon_s N_d$ and a y intercept of $2V_{bi}/q\varepsilon_s N_d$, where V_{bi} is the built-in voltage, V_R is magnitude of the reverse

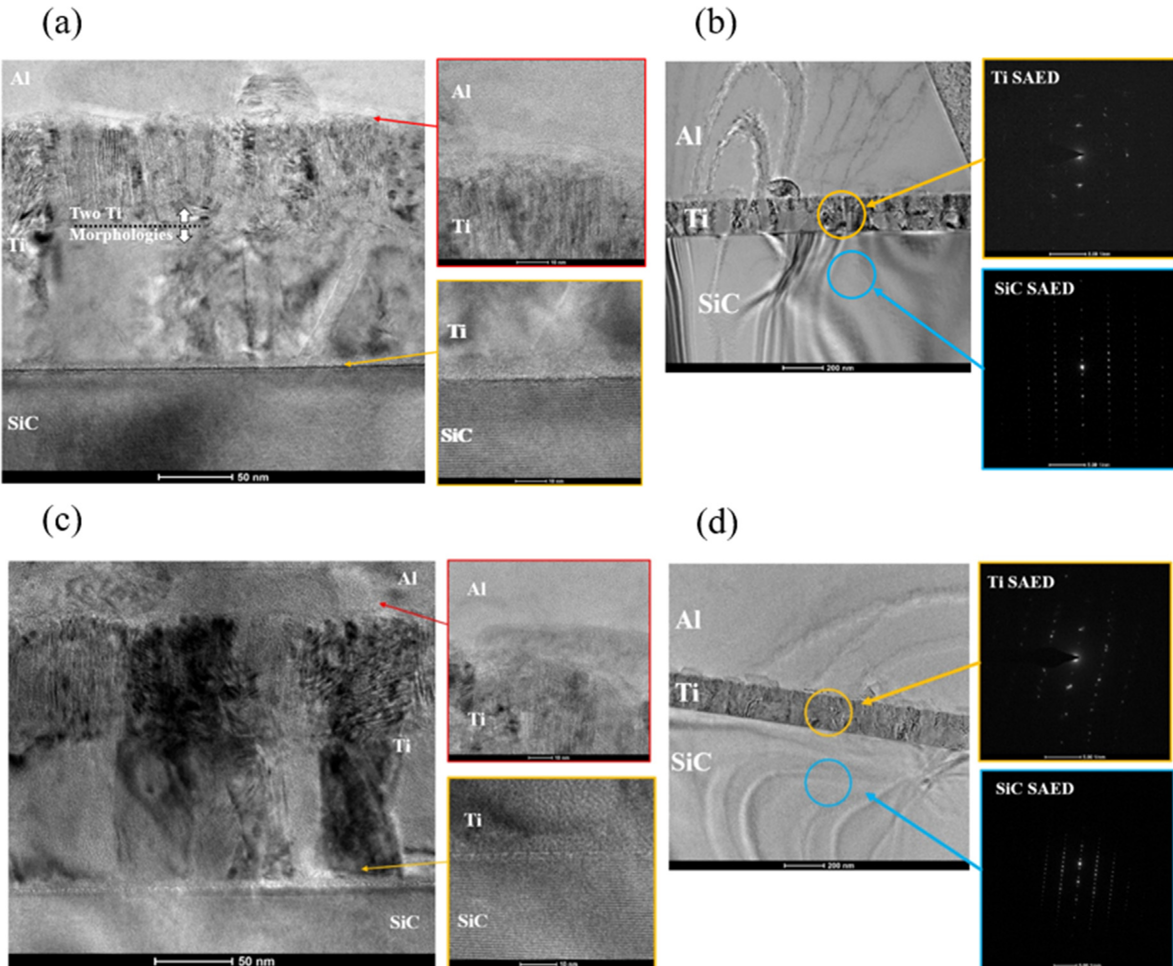

FIG. 4. Microscopic evidence of defect rearrangement in Al/Ti/SiC interfaces with their magnified TEM images and SAED pattern for (a) and (b) electrically degraded and (c) and (d) rejuvenated sample.

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voltage, ε_s is the dielectric constant of the semiconductor, and N_d is the donor dopant concentration. The capacitance depends on the bias and frequency, but the frequency dependence of the C–V data of Ti/4H-SiC is found relatively weak. A slight increase in slope or decrease in N_d is found from $1/C^2$ vs V_R for stressed sample; however, electro pulsing restored the pristine value as shown in Fig. 3(b).

The fundamental principle behind the EWF-based rejuvenation is the enhancement of crystallinity to improve electron transport properties. To get a visual confirmation of crystallinity enhancement, we performed high-resolution transmission election microscopy (HRTEM) on both stressed and annealed samples. Figure 4 shows close-up pictures at the Al/Ti and Ti/SiC interfaces. Interface between Al and Ti is not smooth, rather wavy and intermixed with the Ti layer. The Ti layer is formed on the epitaxial SiC layer, and the transition between metal and semiconductor is smooth and straight. Covalent bond is dominant in SiC, and it is well known that covalent semiconductors have a high density of surface states. Surface states affect the interface behavior and, hence, the device performance. It is important to note the Ti/SiC interface quality for the degraded and rejuvenated phases. High-resolution TEM images in Figs. 4(a) and 4(c) show the interface to be remarkably sharpened after EWF annealing of the stressed sample. The selected area diffraction pattern (SAED) over the Ti/SiC interface for the stressed sample reveals a polycrystalline region (dots and circle in the pattern), whereas EWF annealed sample shows sharp spots indicating crystallinity enhancement in the device. The Ti layer is polycrystalline, and it appears to have two different

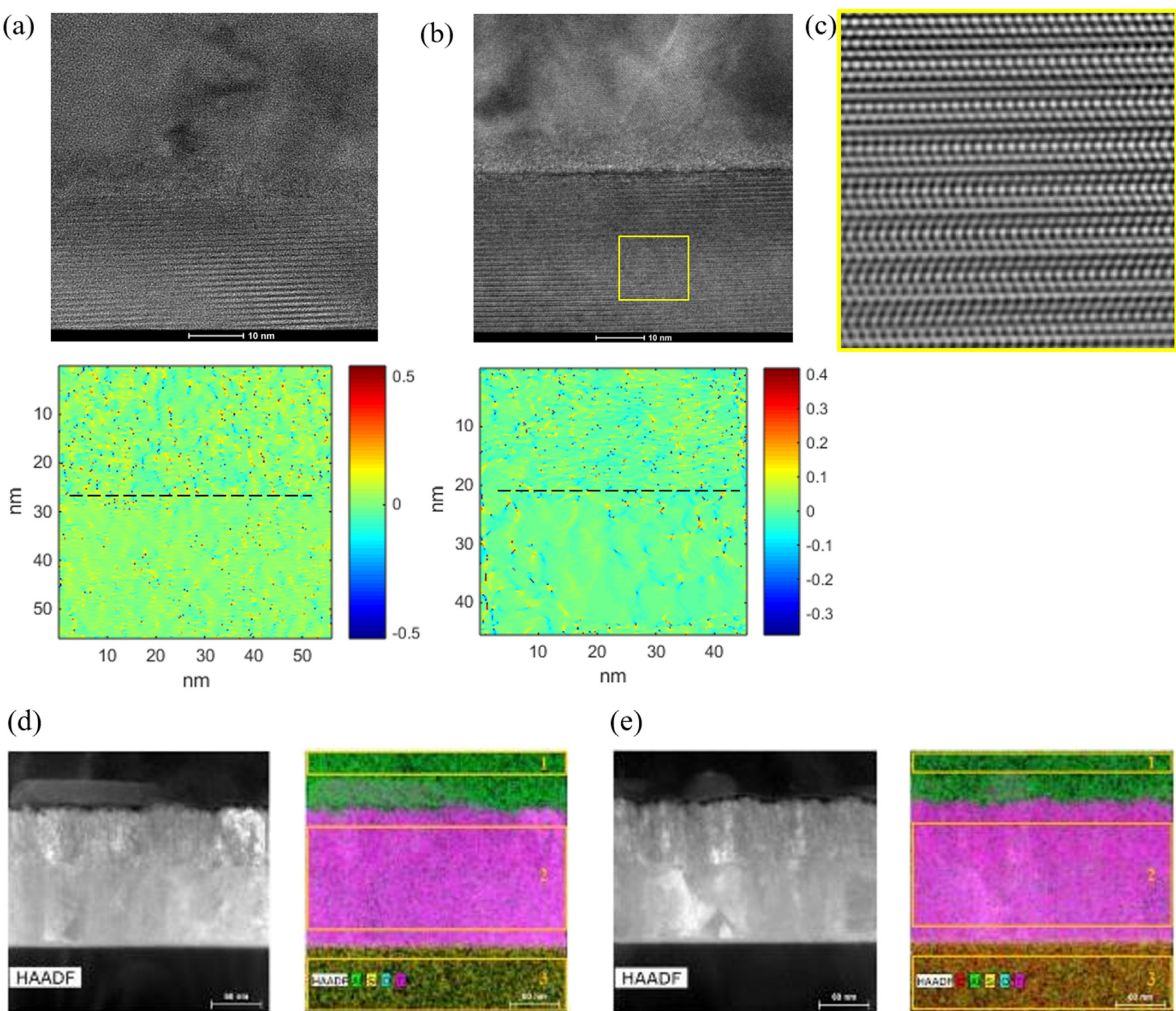

FIG. 5. GPA of HRTEM images and their corresponding strain maps on the SiC layer on (a) electrically degraded and (b) rejuvenated sample. (c) IFFT (Inverse Fast Fourier Transform) filtered image of the yellow bordered region. Each of the neighboring red–blue dots represents the strain field of a dislocation. (d) and (e) High-angle annular dark field images with an elemental map of the Al/Ti/SiC layer for degraded and rejuvenated samples, respectively.

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morphologies on both samples. These morphologies appear as two different layers within the Ti layers shown in Fig. 4(a). The top layer appears more columnar, while the bottom layer exhibits zone 2 or zone 3 grain structures according to the structure zone model, which indicates that the Ti layer may have been deposited in steps.

To highlight the reduction in atomic scale defect density (for the given spatial resolution), we perform geometrical phase analysis (GPA), which can map strain in the device by detecting displacement of atoms in HRTEM images. We filtered the noise from the images by doing an Inverse Fast Fourier Transform (IFFT) and then performed GPA on the IFFT-filtered images in the SiC layer. We notice that both stressed and pulsed SiC contain atomic defects. However, the SiC experiences higher residual strain and defect generation after stressing, as reflected in Figs. 5(a) and 5(b). Electron wind force can impart mobility to the defects and redistribute them and, hence, improve the device performance. Energy dispersive x-ray spectroscopy (EDX) mapping was done in the scanning transmission electron microscopy (STEM) mode to get numerical values (reported in Table I) of the chemical components to check any metal diffusion during high current density electro-pulsing. There is no significant Al or Ti diffusion in the SiC layer, according to Figs. 5(c) and 5(d), although we find that C content is higher in the pulsed sample in region 3 (marked with yellow box). Carbon contamination in STEM is quite common phenomena, which arise due to the hydrocarbon contamination inside TEM.[36] Excess carbon can come from either/both carbon contamination or/and the carbon protective layer used during TEM sample preparation. Oxygen was detected in each layer, but this is most likely a passivation layer formed after exposure to atmospheric conditions after milling as opposed to oxygen present in the bulk.

It is important to note that the TEM analysis in Figs. 4 and 5 are location specific, since only a small coupon is lifted out of the device, and high-resolution microscopy also narrows the field of view. This limitation is difficult to eliminate because it is inherent to higher resolution microscopy. To address this concern, we have performed such analysis at several locations and found consistent reduction in the Schottky barrier region. Microscale x-ray diffraction (XRD) without a title stage was unable to pick signal from the SiC, probably because of the 4° tilt angle epitaxial growth of the single crystal SiC substrate of these devices. This resulted in cutting off the crystal planes of SiC during micro-XRD in a very small area. We performed high-resolution micro-Raman of the stressed and electro-pulsed devices after etching the top metal electrodes of the devices using wet etching technique. These results show relatively higher intensities of the E2 (TO) and A1 (LO) SiC Raman peaks for the electro-pulsed samples suggesting better crystal quality of the electro-pulsed sample compared to the electrically stressed device.

TABLE I. Atomic weight percentage of the chemical element of stressed (gray colored row) and pulsed (white colored row) devices. Regions are defined with the yellow box in Figs. 3(c) and Fig. 3(d).

Region	Al (at. %)	Ti (at. %)	Si (at. %)	C (at. %)	O (at. %)
1	72.37	1.04	0.52	4.55	21.53
	53.22	1.86	0.64	14.88	29.39
2	2.51	73.91	1.66	10.65	11.26
	3.20	59.70	2.01	21.08	14.02
3	5.06	0.65	42.43	44.87	7.00
	4.04	0.77	29.95	58.46	6.78

We demonstrated a room temperature process that takes less than a minute to mitigate defects and improve characteristics of a SiC Schottky barrier diode. The process was performed on intentionally degraded devices. After our rejuvenation process, the electrical output and other performance metrics, such as barrier height and ideality factor, are completely recovered, and even better performance is achieved than pristine condition. TEM imaging with diffraction confirms the quality improvement at both the interfaces and bulk SiC layers. The presence of higher defects and strain in SiC have been reduced after EWF annealing proved from GPA. Also, EDX results show no metal migration after high current injection during stressing and pulsing. Although thermal annealing is a very well-established technique, our room temperature approach can be more beneficial for electronic devices. This is because the process requires only two electrical terminals and there is no need to expose the device to a furnace, laser, or microwave as in classical annealing processes.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

Md Abu Jafar Rasel and Nahid Sultan Al-Mamun contributed equally to this work.

Md Rasel: Conceptualization (equal); Data curation (equal); Formal analysis (equal); Investigation (equal); Methodology (equal); Validation (equal); Visualization (equal); Writing – original draft (equal). **Nahid Sultan Al-Mamun:** Conceptualization (equal); Data curation (equal); Formal analysis (equal); Investigation (equal); Methodology (equal); Validation (equal); Writing – original draft (equal). **Sergei Stepanoff:** Methodology (equal); Validation (equal); Visualization (equal). **Aman Haque:** Conceptualization (equal); Funding acquisition (equal); Project administration (equal); Resources (equal); Supervision (equal); Validation (equal); Writing – review & editing (equal). **Douglas E. Wolfe:** Funding acquisition (equal); Project administration (equal); Supervision (equal); Writing – review & editing (equal). **Fan Ren:** Formal analysis (equal); Funding acquisition (equal); Project administration (equal); Validation (equal); Writing – review & editing (equal). **Stephen J. Pearton:** Formal analysis (equal); Funding acquisition (equal); Investigation (equal); Methodology (equal); Project administration (equal); Writing – review & editing (equal).

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DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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