Article

Annealing Stability of NiO/Ga_2O_3 Vertical Heterojunction Rectifiers

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Abstract: The stability of vertical geometry NiO/Ga_2O_3 rectifiers during two types of annealing were examined, namely (1) the annealing of NiO only, prior to the deposition of the Ni/Au metal anode stack, and (2) the annealing of the completed device. The devices were annealed in oxygen for 1 min at a temperature of up to 500 °C. The results show that annealing at 300 °C can lead to the best performance for both types of devices in terms of maximizing the breakdown voltage and on–off ratio, lowering the forward turn-on voltage, reducing the reverse leakage current, and maintaining the on resistance. The surface morphology remains smooth for 300 °C anneals, and the NiO exhibits a bandgap of 3.84 eV with an almost unity Ni_2O_3/NiO composition.

Keywords: NiO; Ga_2O_3 rectifiers; high breakdown; annealing

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1. Introduction

There has been much recent progress in the development of NiO/β-Ga_2O_3 power rectifiers, with several demonstrations of performance beyond the 1D limit of GaN [1–25]. Currently, the maximum breakdown voltages demonstrated are >8 kV [7,26–28], corresponding to critical fields over 8 MV·cm^{-1}. The exact critical field of β-Ga_2O_3 is generally quoted as ~8 MV·cm^{-1} but is not known to a high level of accuracy and will be dependent on doping in the drift region of rectifiers, temperature, and geometry, all of which influence electric field crowding [29]. Such rectifiers would be applied in higher voltage switching systems, which are critical components of distributed energy resources, electric vehicle drive trains and charging infrastructure, and more efficient motor drives [30].

While the dc breakdown and switching performance of the se rectifiers has been established [2–7], one aspect of the performance that has received less attention is stability during annealing. Thermal stability plays a crucial role in the performance and reliability of gallium oxide (Ga_2O_3) power devices, making it an essential characteristic for their successful operation. Ga_2O_3 power devices are known for their exceptional power handling capabilities, high breakdown voltages, and wide bandgap properties. However, these devices are subjected to considerable heat generation during operation due to the substantial power dissipation associated with high-current and high-voltage applications. The thermal stability of Ga_2O_3 power devices becomes paramount as it directly impacts their efficiency, lifespan, and overall performance. Efficient heat dissipation and thermal management are imperative to prevent excessive temperature rise, which can lead to device degradation, increased leakage current, and even catastrophic failure.

The surface morphology of contacts is important in gallium oxide power devices because it can affect the following:

Schottky barrier height: The Schottky barrier height is the energy difference between the Fermi level of the metal contact and the conduction band of the semiconductor. A high Schottky barrier height is desirable for power devices because it leads to a low on-resistance.

The surface morphology of the contact can affect the Schottky barrier height by changing the density of the surface states at the interface.

Contact resistance: The contact resistance is the resistance between the metal contact and the semiconductor. A low contact resistance is desirable for power devices because it leads to a low power loss. The surface morphology of the contact can affect the contact resistance by changing the area of contact between the metal and the semiconductor.

Coulomb scattering: Coulomb scattering is a type of scattering that occurs when electrons interact with the electric field of charged impurities at the semiconductor's surface. Coulomb scattering can increase the resistivity of the semiconductor and lead to a decrease in the device's performance. The surface morphology of the contact can affect Coulomb scattering by changing the density of charged impurities at the surface.

In general, a smooth, atomically flat surface is desirable for gallium oxide power devices because it leads to a high Schottky barrier height, a low contact resistance, and a low density of charged impurities. However, it is difficult to achieve a perfectly smooth surface in practice, so the surface morphology of the contact is often optimized to achieve a balance between these different factors.

The following are some of the methods that can be used to improve the surface morphology of contacts in gallium oxide power devices:

Annealing: Annealing the contact can help to smooth out the surface and reduce the density of the defects.

Chemical cleaning: Chemical cleaning can remove surface contaminants that can degrade the contact performance.

Ion implantation: Ion implantation can be used to introduce dopants into the semiconductor's surface, which can improve the Schottky barrier height and reduce the contact resistance.

Atomic layer deposition (ALD): ALD can be used to deposit a thin layer of a dielectric material on the contact surface, which can help to reduce Coulomb scattering and improve the device's performance.

The development of new methods for improving the surface morphology of contacts in gallium oxide power devices is an active area of research. As these methods are improved, it is expected that the performance of gallium oxide power devices will continue to improve. By ensuring excellent thermal stability, Ga_2O_3 power devices can maintain optimal performance, minimize thermal-induced stresses, and enhance their overall reliability, thereby enabling their seamless integration in various power electronics applications. It is common to anneal the NiO at low temperatures to optimize the hole density in these layers [28], but a detailed study of the effect of the metal stack on top of the NiO and an extended range of annealing temperatures has not been reported. In this paper, we examine the effect of either annealing the NiO alone or annealing the whole device at temperatures of up to 500 °C. We found that annealing at 300 °C produced the best performance for both types of devices.

2. Materials and Methods

A schematic of the vertical rectifier structures is shown in Figure 1 (left). The fabrication has been described in detail elsewhere [25–27]. In summary, we employ a bilayer of NiO in order to maximize both breakdown voltage and current spreading while minimizing on-state resistance, R_{ON}. The NiO bilayer thickness is 10/10 nm and the NiO is extended beyond the Ni/Au anode contact extension by 8 μm to form guard rings. The 10 μm thick drift layer was grown via halide vapor phase epitaxy (HVPE) on a (001) Sn-doped (10^{19} cm^{-3}) bulk β-Ga_2O_3 single crystal substrate. The X-ray diffraction (Rigaku, Tokyo, Japan) full width at half maximum (FWHM) of this substrate is <350 arc·sec in both [100] and [010] directions, and its thickness is 650 μm, as supplied by the manufacturer. The backside Ohmic contacts were deposited via e-beam evaporation of Ti/Au. The contact was annealed at 550 °C for 180 s under flowing N_2 atmosphere. Surface engineering and interlayer materials were investigated to mitigate metal diffusion and improve adhesion between the metal and Ga_2O_3. Alloyed metal contacts, such as Ni/Au- or Ti/Al-based

systems, have shown improved thermal stability, reducing contact resistance over extended temperature ranges.

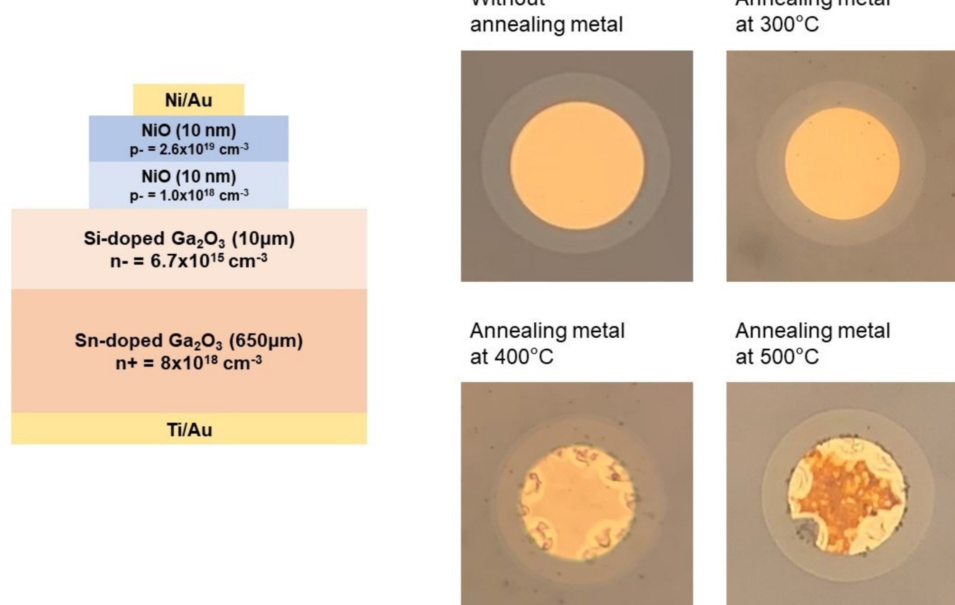

Figure 1. Device structure (**left**) and optical images after annealing at various temperatures (**right**).

We employ a low power during the rf sputter deposition of the NiO bilayers that form the heterojunction [27]. The deposition was carried out via rf (13.56 MHz) magnetron sputtering at 3 mTorr [28]. Finally, a cathode contact of 20/80 nm Ni/Au (100 µm in diameter) was deposited onto the NiO layers. We annealed the devices under flowing O_2 ambient for 1 min at temperatures of up to 500 °C, either before or after the deposition of the Ni/Au anode metal stack. The anneals were performed in a conventional rapid thermal annealing system. The devices were placed on a Si wafer, with the temperature monitored by a thermocouple, and the heating and cooling rates were of the order of 50–80 °C per second.

The current density–voltage (J–V) characteristics, representing current density as a function of voltage, were obtained through measurements conducted using a Tektronix 370-A curve tracer, 371-B curve (Tektronix, Beaverton, OR, USA), and Agilent 4156C (Agilent Technologies, Santa Clara, CA, USA). The reverse voltage characteristics were measured using a Glassman power supply, which has an upper limit of 10 kV. The reverse breakdown voltage was determined by identifying the bias at which the reverse current reached 0.1 A·cm^2. This is a common definition of breakdown in such devices. High bias measurements were conducted within a Fluorinert atmosphere. Under these conditions, the devices did not incur permanent damage. This atmosphere allows for the application of high voltages without the breakdown that would occur in air ambient. However, increasing the voltage by an additional 50–200 V resulted in irreversible failure due to breakdown at the contact periphery. The on-resistance values were calculated based on an assumed current spreading length of 10 µm and a spreading angle of 45°. Additionally, the resistance contributed by the cable, probe, and chuck, which amounted to approximately 10 Ohm, was subtracted from the calculations. The doping concentration in the drift layer was determined from capacitance–voltage (C–V) data obtained at a frequency of 100 kHz and series mode.

3. Results

It is important to point out that the annealing up to 500 °C did not affect the structural properties of the epitaxial layer structure. The thermal stability of the beta polytype

β-Ga_2O_3 plays a critical role in determining its applicability in advanced electronic and optoelectronic devices [28,29]. With its stable crystal structure, high thermal conductivity, and remarkable resistance to elevated temperatures, β-Ga_2O_3 holds great promise for future technological advancements in the field of solid-state devices. The investigation of β-Ga_2O_3's thermal properties is crucial to ascertain its viability in high-temperature applications. Studies have shown that β-Ga_2O_3 exhibits excellent thermal conductivity, aiding in efficient heat dissipation. Moreover, its high melting point, which is estimated to be around 1900 °C, further underscores its thermal stability. The β-Ga_2O_3 crystal structure belongs to the monoclinic space group C2/m, consisting of stacked GaO_6 octahedra forming double layers [29]. These layers are interconnected through van der Waals forces, resulting in a stable crystal lattice. Under specific temperature conditions, β-Ga_2O_3 undergoes phase transitions to other polymorphs, such as the alpha (α), gamma (γ), and epsilon (ε) phases [29]. However, the β phase remains stable at temperatures of up to approximately 1000 °C. Thus, our annealing to 500 °C does not affect the crystal quality of our epitaxial structure, and all changers are due to the thermal stability of the NiO and metal contacts. Further research and experimentation are essential to fully explore and optimize its potential in practical applications.

In terms of the effect of annealing on the devices, we began by examining the surface morphology for devices after annealing either with or without the Ni/Au metal stack in place. There is little information available on the thermal stability of metals on NiO.

The surface morphology of the devices after annealing with the anode metal in place is shown in the optical images at the right of Figure 1. Notice that obvious degradation is present after 400 °C annealing, with catastrophic damage after 500 °C annealing. For contacts on NiO, Ni/Au contacts are commonly used as Ohmic contacts due to their low resistivity and stable electrical behavior. Understanding their thermal stability is essential to ensure good device performance under varying temperature conditions.

Research has shown that Ni/Au contacts on NiO undergo temperature-induced changes, affecting their electrical properties and contact resistivity. At elevated temperatures, the diffusion of Ni and Au atoms into the NiO semiconductor layer can occur, leading to the formation of nickel oxide compounds and alloying with the Au layer. These interfacial reactions can alter the metal–semiconductor interface, degrading the Ohmic behavior and increasing contact resistivity.

To mitigate these issues, researchers have explored different strategies to enhance the thermal stability of Ni/Au contacts on NiO. Thin barrier layers, such as titanium or titanium nitride, were introduced between the Ni/Au and NiO layers to inhibit metal diffusion and improve adhesion. Additionally, alloying Ni and Au can create intermetallic compounds that offer improved thermal stability compared to pure metals.

Characterization techniques like current–voltage (IV) measurements and temperature-dependent IV analysis have been employed to assess the thermal stability of Ni/Au contacts on NiO. These analyses aid in understanding the changes in electrical behavior as a function of temperature, helping to optimize contact design for reliable device performance.

In conclusion, investigating the thermal stability of Ni/Au contacts on NiO is crucial for the successful implementation of NiO-based electronic devices. Addressing the challenges related to interfacial reactions and metal diffusion is vital to ensure long-term device reliability and performance under varying temperature environments. Advancements in contact materials and design are continuously being pursued to achieve enhanced thermal stability and enable the full potential of NiO for various electronic applications.

By sharp contrast, the NiO itself did not show significant surface roughening after these anneals. The thermal stability of these thin films is paramount for sustaining functionality under operating conditions involving elevated temperatures. Thermal stability studies of NiO thin films provide insights into their structural integrity and electro-optical characteristics, paving the way for improved material design and device fabrication. Previous work has investigated the effects of temperature on crystal structure. Under varying temperature conditions, NiO thin films may undergo structural changes, impacting their

performance. Researchers have found that at room temperature, NiO thin films typically adopt the antiferromagnetic rock salt structure (B1 phase). However, at elevated temperatures, these films may experience phase transformations, such as the transition to the face-centered cubic (FCC) structure (B2 phase). The reversibility of such transformations and their impact on the material properties are essential considerations for improving device stability.

In terms of microstructural evolution, the thermal stability investigations have also encompassed the microstructural evolution of NiO thin films under heat exposure. At elevated temperatures, grain growth and diffusion processes within the film affect its microstructure, grain boundaries, and surface morphology. The understanding of these phenomena is crucial for optimizing film quality and long-term performance.

In terms of changes in electrical properties, the temperature-induced changes in the electrical properties of NiO thin films are of great interest in electronic device applications. The impact of thermal annealing on electrical conductivity, carrier mobility, and carrier concentration can significantly influence device performance and reliability. Therefore, comprehensive studies on the temperature-dependent electrical characteristics are essential.

Finally, the effect of annealing on phase transitions is also important. NiO thin films exhibit diverse phase transitions under different thermal conditions. Understanding the critical temperatures at which these phase transitions occur is vital for controlling material behavior and tailoring its properties to specific applications. In conclusion, the thermal stability of nickel oxide (NiO) thin films is a multidimensional aspect that profoundly influences their performance and applicability in various technological fields. Investigations into the effects of temperature on the crystal structure, microstructure, electrical properties, and phase transitions of NiO thin films are essential for optimizing their functionality and reliability. By addressing the challenges associated with thermal stability, researchers and engineers can unlock the full potential of NiO thin films for advanced applications, including catalysis, sensing, optoelectronics, and energy storage systems. Future research efforts should focus on further elucidating the underlying mechanisms governing thermal stability and developing strategies to enhance the robustness of NiO thin films under diverse operating conditions.

Table 1 summarizes the RMS measured via atomic force microscopy, along with the resistivity, bandgap, density, and compositional changes. Annealing at 400 °C or above leads to the NiO becoming highly resistive compared to its as-deposited state, while the average bandgap is determined via Tauc plots of absorbance using a UV-Vis spectrometer [28]. We have previously reported that this is a result of a higher oxygen content, which is consistent with the annealing under the O_2 ambient [28]. The bandgap decreases as the Ni_2O_3 ratio in the films decreases [30]. This is consistent with the trend as a function of the O_2/Ar ratio during deposition and suggests that a higher annealing temperature causes a loss of oxygen. From Table 1, it is clear that a post-deposition anneal at 300 °C under O_2 produces the optimum NiO properties. The hole concentration in NiO is determined by the oxygen partial pressure in sputtering. The p-NiO anode layer contributes very little to the on-state resistance of the rectifier.

Table 1. Composition, resistivity, energy bandgap, density, and RMS roughness data for films as a function of postdeposition annealing temperature.

	Ni_2O_3/NiO	Resistivity (Ω·cm)	E_g (eV)	Density (g/cm^3)	Roughness (nm)
As-dep.	1.77	2.79	3.90	5.50	-
300 °C	1.08	5.6	3.84	5.72	0.597
400 °C	1.01	>10	3.76	5.75	1.083
500 °C	0.63	>10	3.74	5.96	0.989

Figure 2 shows the forward I–V characteristics from the devices annealed at different temperatures either without (left) or with (right) the Ni/u contact in place on top of the NiO, along with the corresponding R_{ON} values. The latter were in the range of 7.1–7.8 mΩ·cm^2

for the as-deposited devices and were relatively unaffected by annealing up to 300 °C. At higher temperatures, the R_{ON} was degraded for both types of anneals, due to the increase in resistivity of the NiO and the degraded metal in the case of annealing with the Ni/Au in place. Note the large increase in the low-bias forward current for annealing at or above 400 °C, which is consistent with the increase in recombination centers in the heterojunction [3,30–32].

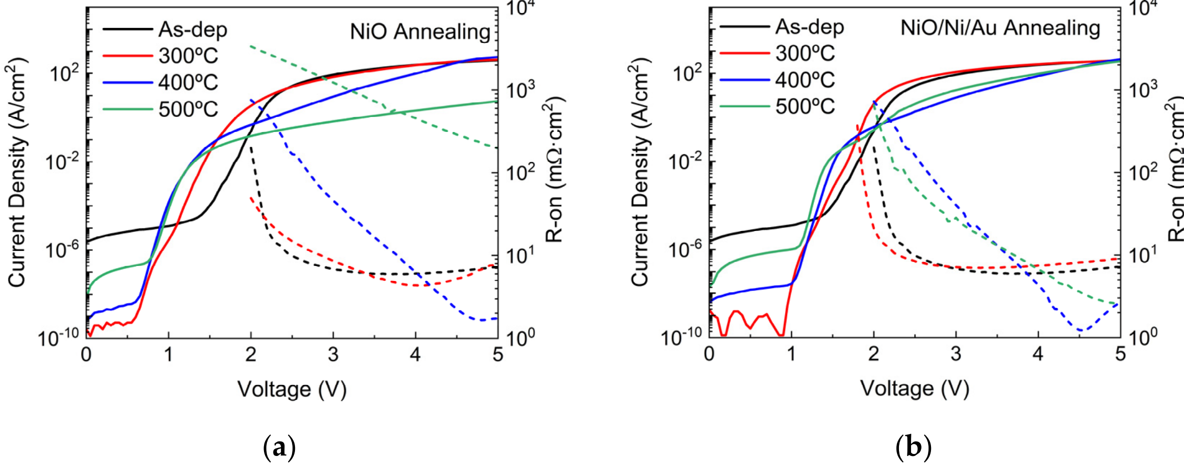

Figure 2. Forward current densities and R_{ON} values for devices with (**a**) annealed NiO and (**b**) annealed NiO/contact metal as a function of temperature.

The turn-on voltages were derived from the linear plots of the forward current density as a function of voltage and are shown in Figure 3. The turn-on voltage marks the point of significant current flow and is dependent on the doping of both sides of the junction. Since annealing causes a reduction in the conductivity of the NiO, the turn-on voltages are degraded at high annealing temperatures. Once again, the devices are stable for anneals of up to 300 °C, but higher temperatures degrade the turn-on voltages. The R_{ON} of the rectifiers is dominated by the drift region resistance. Callahan et al. [33] reported the contact resistance of Ohmic contacts to n-type layers fabricated using an ultra-thin layer of Ti (5 nm) with a Au capping layer (100 nm); they exhibited remarkable stability and Ohmic performance even after thermal cycling to 550 °C and long-term thermal soaking at 600 °C for a minimum of 500 h under vacuum conditions. The TEM revealed that the 5 nm Ti layer underwent a complete transformation into an epitaxial, highly conductive anatase titanium oxide layer, which resulted in a stable Ohmic contact [34,35]. In contrast, the 10 nm Ti layer did not fully react, leading to the formation of a partially amorphous TiOx layer that could not support a stable Ohmic contact. Both the 5 nm and 10 nm Ti samples showed the presence of Ti on the outer surface of the Au layer. However, the homogeneity of the interlayer at the Ga_2O_3 interface was found to have a more significant impact on the overall performance and stability of the fabricated Ohmic contacts. Lee et al. [36] found that the optimum contact resistance of Ti/Au was obtained at 420 °C, superior to the commonly used 470 °C for (010)-oriented Ga_2O_3. However, a significant degradation in the Ohmic contact properties was observed when the anneal temperature was increased to 520 °C, resulting in a contact resistance of ~1.36×10^{-3} $\Omega \cdot cm^2$. A microscopic analysis of the degraded Ohmic contact revealed the formation of $GaAu_2$ inclusions between the (310)-Ga_2O_3 planes and the Ti–TiOx interfacial layer, which expanded to a thickness of 25–30 nm. This deterioration was attributed to the excessive in-diffusion of Au and the out-diffusion of Ga, accompanied by the expansion of the Ti–TiOx layer. The observed contact degradation occurred under relatively moderate annealing conditions (520 °C for 1 min), indicating the urgent need to explore alternative metallization schemes for gallium oxide, potentially including the use of Au-free electrodes [36].

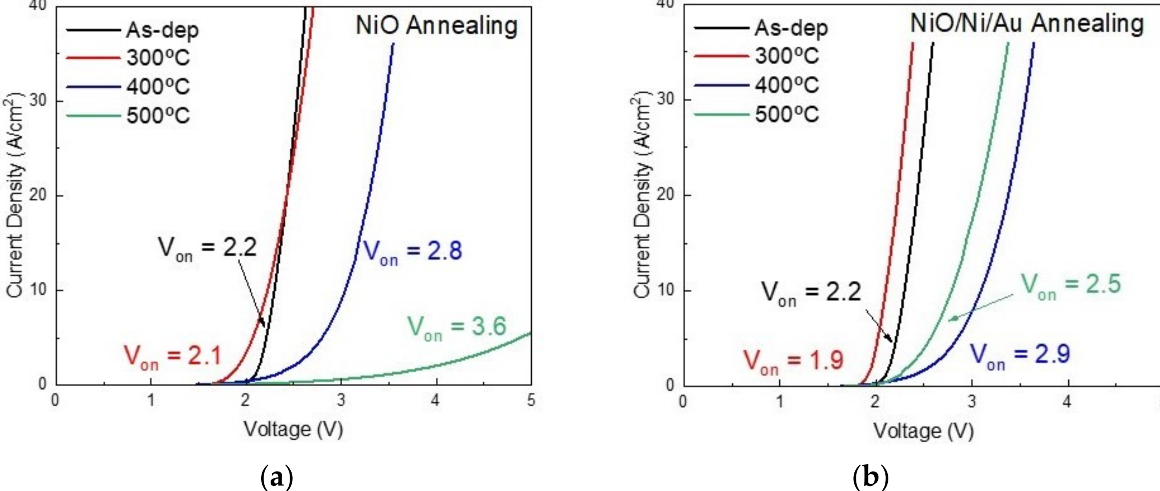

Figure 3. Forward turn-on voltage for devices with (**a**) annealed NiO and (**b**) annealed NiO/contact metal as a function of temperature.

The low-bias reverse current density characteristics are shown in Figure 4 for the devices annealed under the two different processes. The current decreases by 4–5 orders of magnitude for anneals at 300 °C but degrades for higher annealing temperatures. Note that they still do not reach the values on the unannealed rectifiers, signifying that some heat treatment of the devices is necessary to achieve optimum performance. Since the resistivity of the 300 °C annealed NiO films have slightly higher resistivities, this cannot be due to the improved current spreading, but must relate to a reduced defect concentration after annealing. The reverse leakage current density still follows a ln(J) ∝ V relation independent of the annealing condition, which suggests that the main leakage mechanism is still electron variable-range-hopping via defect-related states in the drift region [3], but with a lower leakage contribution from the p-side of the junction.

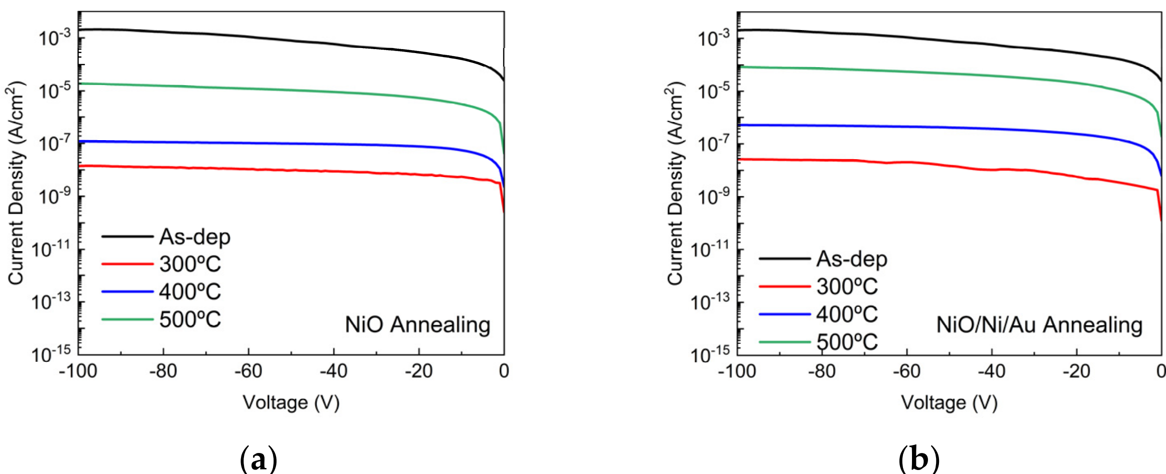

Figure 4. Reverse J–V characteristics for devices with (**a**) annealed NiO and (**b**) annealed NiO/contact metal as a function of temperature.

In Figure 5, we present the diode on–off ratio for devices after both types of annealing. The on–off ratio is defined as the ratio that is observed when transitioning from a forward voltage of +10 V to reverse voltages ranging from 0 V to −100 V, as indicated on the x-axis. The heterojunction diodes exhibit an on–off ratio of over 1010 after heat treatment at 300 °C for both types of annealing within the voltage range of 0 V to −100 V. This is slightly higher

than for the unannealed cases. For annealing at 400 °C and higher, the on–off ratios degrade by more than 4 orders of magnitude.

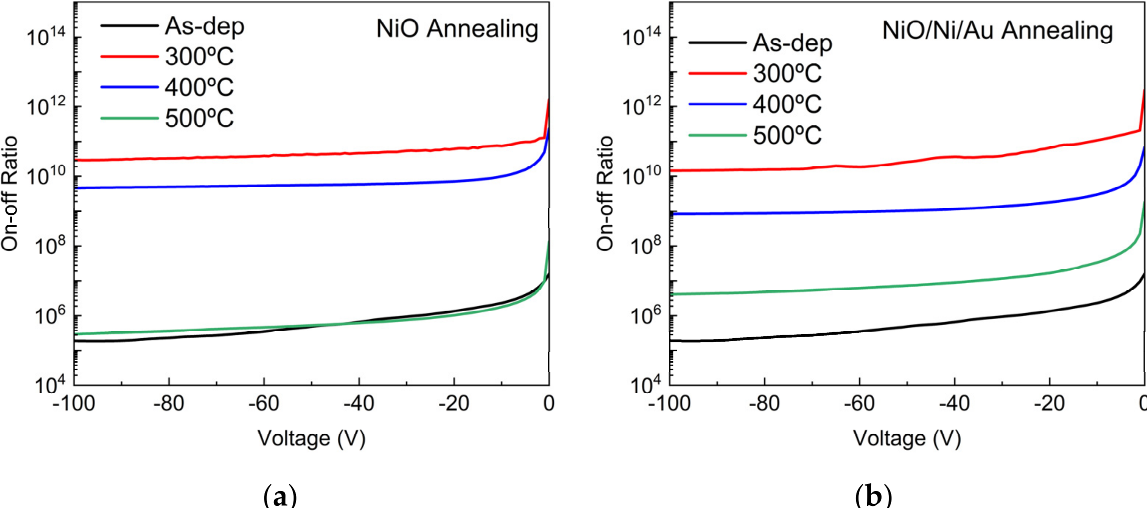

Figure 5. On–off ratios for devices with (**a**) annealed NiO and (**b**) annealed NiO/contact metal as a function of temperature.

Note that the on–off ratio is another figure of merit for Ga_2O_3 in that having a high on-current and low leakage current in reverse bias is favorable for switching applications. We found in our devices that the reverse recovery time of ~21 nanosecs was independent of temperature over the range of up to 300 °C. This is defined as the time required to reach 25% of the peak current.

The reverse J-V characteristics over the full bias range are shown in Figure 6 for the devices annealed in both sequences at different temperatures. The key points from this data are, firstly, that the V_B increases by ~50% after 300 °C annealing in both cases. The second point is that the use of higher annealing temperatures of the heterojunction really decreases the V_B, but they remain above the unannealed value even after annealing at 500 °C.

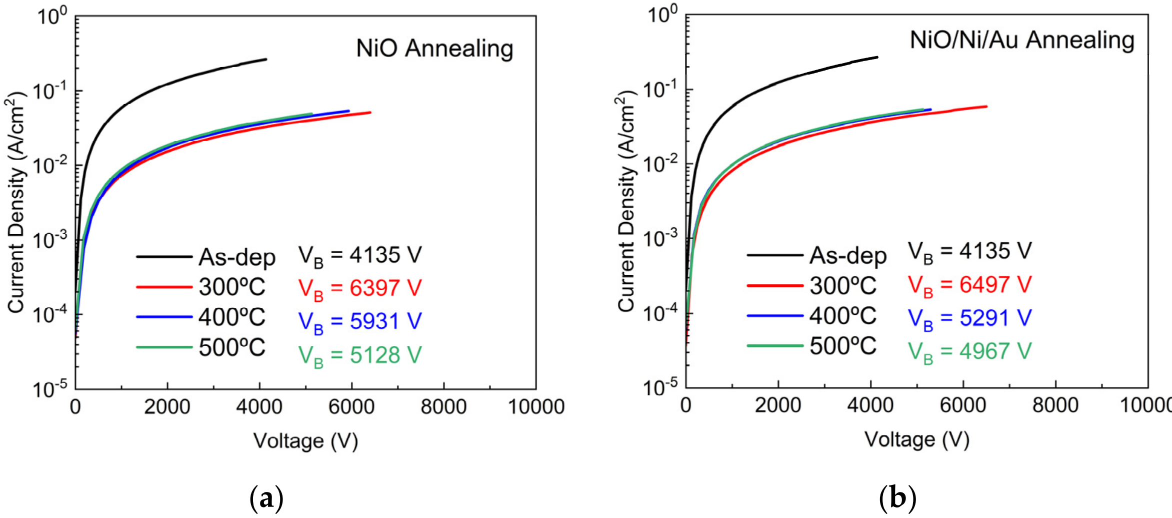

Figure 6. Reverse J–V characteristics for devices with (**a**) annealed NiO and (**b**) annealed NiO/contact metal as a function of annealing temperature.

Figure 7 shows a comparison of the breakdown voltages for the devices annealed in the two different sequences. The power figure of merit $V_B{}^2/R_{ON}$ was 6.47 GW·cm^{-2} for

the 300 °C annealing, which optimized the anneal heterojunction rectifier, compared to 3.49 GW·cm^{-2} for the unannealed case. The theoretical maximum is ~34 GW·cm^{-2} [7], showing that there remains room for the continued optimization of both materials, device design, and processing steps.

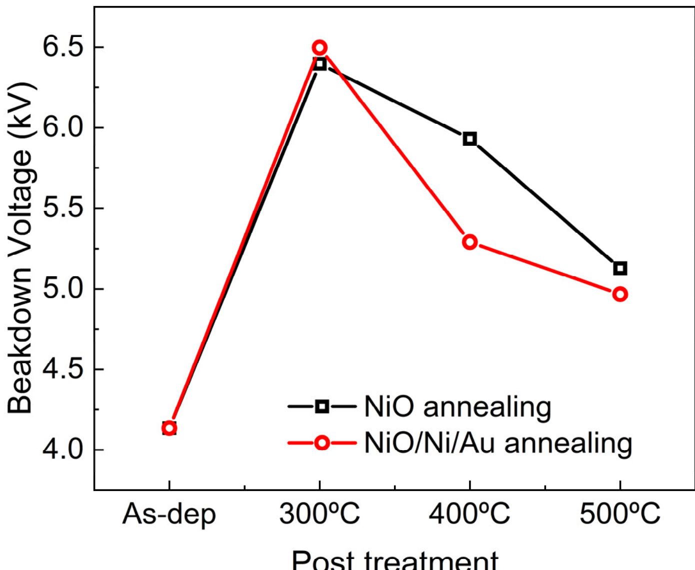

Figure 7. Breakdown voltages as a function of annealing temperature for annealing with either the NiO or the NiO/contact metal stack.

4. Conclusions

The annealing temperature in this study was chosen based on previous studies that have shown that NiO/Ga_2O_3 rectifiers exhibit an optimal performance at around 300 °C. There is no significant change in the crystalline quality, carrier density, or mobility for annealing up to 500 °C [31–36], which is the temperature we used in our experiments. At slightly higher temperatures, there can be changes in the metal contacts used on the device structure and in the NiO layers. The surface Fermi level can change with annealing in undoped layers due to the removal of adsorbates, but little change is expected in the doped layers [37]. The annealing of the NiO layer in the NiO/β-Ga_2O_3 vertical rectifiers was found to improve the device characteristics, with an increase in the breakdown voltage and the power figure of merit for the optimized condition of 300 °C. This improvement occurs independent of whether this is performed on the NiO prior to the deposition of the anode metal or after the deposition of the metal stack. The anneal under the O_2 ambient was found to reduce the junction leakage current through a reduction in the defect density in the NiO. Annealing at 400 °C or above was found to lead to a degradation in the breakdown and on-state resistance, but the values remained above those for the nonannealed devices.

There are still open questions with the thermal stability of Ga_2O_3 devices. One issue is that Ga_2O_3 can undergo a phase transition from the β-phase to the α-phase at high temperatures. The α-phase is less stable than the β-phase, and it can lead to a degradation of the device's electrical properties. This phase transition can be triggered by a number of factors, including high temperature, high electric field, and ion irradiation.

Another issue with the thermal stability of Ga_2O_3 devices is that they can be susceptible to oxidation. This can lead to the formation of a surface layer of gallium oxide hydroxide (GaOOH), which can degrade the device's performance. The oxidation of Ga_2O_3 can be accelerated by high temperature, high humidity, and the presence of certain impurities. There are a number of ways to address the thermal stability issues of Ga_2O_3 devices. One approach is to use a buffer layer between the Ga_2O_3 and the metal contacts. This buffer layer can help to prevent the diffusion of metal atoms into the Ga_2O_3, which can lead to the formation of the α-phase. Another approach is to use a passivating layer on the

surface of the Ga_2O_3. This passivating layer can help to protect the Ga_2O_3 from oxidation. There is still some research that needs to be conducted to fully understand the thermal stability of Ga_2O_3 devices. However, the progress that has been made so far is promising. With continued research, Ga_2O_3 can become a viable alternative to other semiconductor materials for power electronic devices.

In addition to the two issues mentioned above, there are a few other remaining issues with the thermal stability of Ga_2O_3 power electronic devices. One issue is that Ga_2O_3 can be susceptible to thermal runaway. This is a self-accelerating process in which the temperature of the device increases, which, in turn, leads to an increase in the current flow, which further increases the temperature. This can cause the device to melt or explode.

Another issue is that Ga_2O_3 devices can be susceptible to hot carrier degradation. This is a process in which high-energy electrons damage the material's crystal structure. This can lead to a decrease in the device's performance and a shortened lifespan. Despite these remaining issues, Ga_2O_3 is a promising material for power electronic devices. The high thermal conductivity of Ga_2O_3 can help to dissipate heat, which can help to prevent thermal runaway and hot carrier degradation. Additionally, the high breakdown voltage of Ga_2O_3 can allow for devices to operate at higher voltages, which can lead to improved efficiency. With continued research, the thermal stability of Ga_2O_3 power electronic devices is likely to improve. As this happens, Ga_2O_3 is expected to become a more widely used material for these devices.

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