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ABSTRACT

Sputtered p-NiO films were used to suppress gate leakage and produce a positive shift in the gate voltage of AlGaN/GaN high-electron mobility transistors for e-mode operation. A direct comparison with Schottky-gated devices fabricated on the same wafer shows the utility of the NiO in increasing the on-off ratio and shifting the threshold voltage from −0.95 V (Schottky gated) to +0.9 V (NiO gated). The breakdown voltage was 780 V for a 40 μm drain-source separation. The subthreshold swing decreased from 181 mV/dec for Schottky-gated HEMTs to 128 mV/dec on NiO-gated devices. The simple fabrication process without any annealing or passivation steps shows the promise of NiO gates for e-mode AlGaN/GaN HEMT operation.

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I. INTRODUCTION

The use of p-NiO layers in the gate structure of AlGaN/GaN high electron mobility transistors (HEMTs) shows promise as a method for depleting the 2DEG in the channel to obtain a normally off operation.[1–11] Compared with other approaches, no etching is needed to control the threshold voltage, and an absence of Mg diffusion is an issue in the more generally used p-GaN layers.[12] The doping and bonding in the NiO layers have been controlled by the initial deposition parameters or by postdeposition annealing.[2,6] In some cases, Li-doping of the NiO has been used to tune the band alignment with the underlying AlGaN.[3] Trigate GaN junction HEMTs were demonstrated using a p-type NiO in which the gate metal formed an Ohmic contact with NiO.[4] The resulting devices exhibited minimal hysteresis with a low subthreshold slope of 63 mV/dec with a high on-off current ratio of 10^8.[4] Guo *et al.* reported p-NiO-gated HEMTs with a breakdown voltage of 1200 V and specific on-resistance of 2.22 mΩ cm^2, producing a Baliga's figure-of-merit of 0.65 GW/cm^2. However, these devices required gate etching and postannealing at 450 °C.[7] The valence and conduction band offsets with AlGaN are in the range of 1.6–2.9 and 1.4–2.4 eV,[11,13] respectively, providing excellent carrier confinement.

It is desirable to simplify the NiO approach to obtaining e-mode operation to make it competitive with other approaches such as the use of p-GaN gates or recessed gate structures.[14–21] These structures still have issues such as threshold voltage instabilities due to electron trapping or charge storage effects.[22–30]

One drawback of the sputtered NiO approach has been the need for performing relatively high-temperature annealing in some cases (350–500 °C) to optimize the NiO properties,[1–7] but we have found that this problem can be solved by controlling the initial deposition conditions. In this paper, we show that no postdeposition annealing of NiO is needed to produce low-hysteresis, e-mode HEMTs and that stable operation is achieved without surface passivation. This simplified fabrication process makes this approach attractive for e-mode HEMT applications.

II. EXPERIMENT

The HEMT structure is shown in Fig. 1. The epitaxial structure grown by metal organic chemical vapor deposition on a semi-insulating 4H-SiC substrate consists of a 2 μm, lower-growth temperature GaN buffer, a 55 nm undoped GaN channel, a 2 nm undoped $Al_{0.25}Ga_{0.75}N$, and a 1 nm GaN cap. The Ohmic contacts (Ti/AI/Ni/Au, annealed 850 °C, 30 s) and Schottky metal gate electrodes (Ni/Pt/Au) were formed by electron beam evaporation and lift-off of the metallization. We formed both Schottky-gated and NiO-gated devices on the same wafer, with a gate length of 200 μm, a drain-source separation of 10–40 μm, and a gate length of 1 μm.

The NiO layers, which were 25 nm in total thickness, were deposited by magnetron sputtering in a system from Kurt Lesker.

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The process occurred at a working pressure of 3 mTorr with a power of 150 W and a radio frequency of 13.56 MHz, using dual targets to reach a deposition speed of approximately 2 Å s^{-1}.[30] An O_2/Ar gas mixture with a ratio of 1:10 was used, resulting in polycrystalline films that exhibited a bandgap of 3.75 eV, a resistivity of 0.1 Ω cm, and a density of 5.6 g cm^{-3}.[31]

For scanning transmission electron microscopy (STEM) studies, cross-sectional samples were prepared by a standard *in situ* focused ion beam (FIB) thinning procedure using a FEI Helios Nanolab 600I dual beam FIB/scanning electron microscopy (SEM) with a Ga ion source. High-angle annular dark-field scanning transmission electron microscopy (HAADF-STEM) imaging was performed using an aberration-corrected Themis Z STEM (Fisher Scientific). Elemental analysis was performed using energy-dispersive x-ray spectroscopy (EDS) on the Themis Z equipped with a SuperX detector system.

The DC and pulse-mode device characteristics consisting of the drain current-voltage (I–V), forward and reverse gate I–V, and transfer characteristics were measured with an HP 4156 parameter analyzer at 25 °C. The breakdown voltages were examined by using a Tektronix curve tracer 371B.

III. RESULTS AND DISCUSSION

A low-magnification HAADF-STEM image showing the complete film stack with the gate contact and protective Pt layer on top is shown in Fig. 2(a). Damage at the bottom NiO interface is observed, which is likely due to sputtering-related damage. A high-magnification HAADF-STEM image in Fig. 2(b) reveals atomically abrupt interfaces from the GaN cap to the GaN channel with no extended defects observed. Note that the higher contrast in GaN is due to the higher atomic number (Z) of Ga (Z = 31) relative to that of Al (Z = 13). The corresponding atomic model of the GaN crystal structure is shown in Fig. 1(c) for the [21$\bar{3}$0] zone axis. In Fig. 2(d), a lower-magnification HAADF-STEM image is shown where the EDS acquisition was performed. The EDS line profile from the red arrow in Fig. 2(d) is shown in Fig. 1(e), indicating the correct film stack ordering.

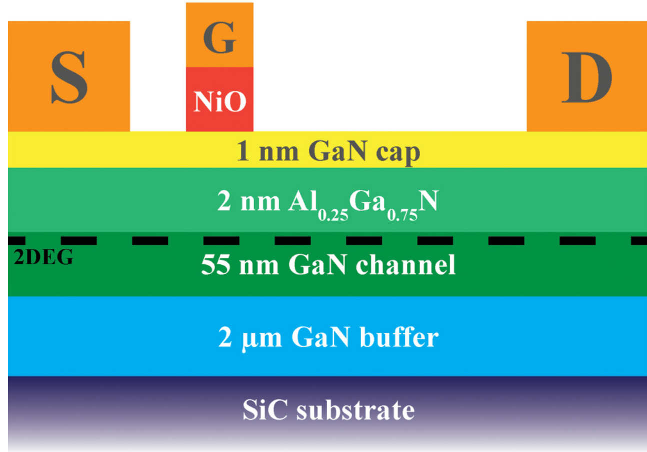
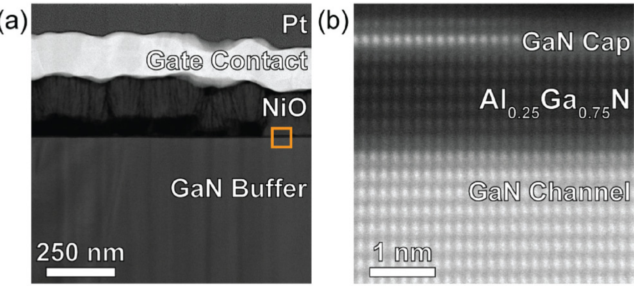
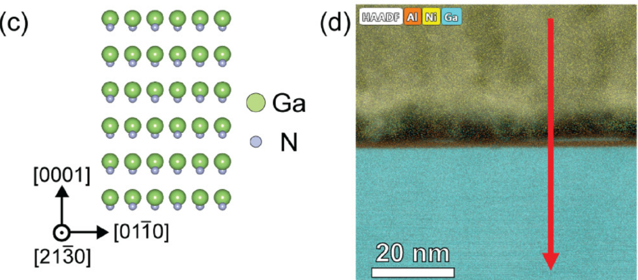


FIG. 1. Schematic of an NiO/AlGaN/GaN HEMT structure. The gate length is 200 µm, the source-drain distances are 10–40 µm, the gate length is 1 µm, and the thickness of the NiO is 25 nm.





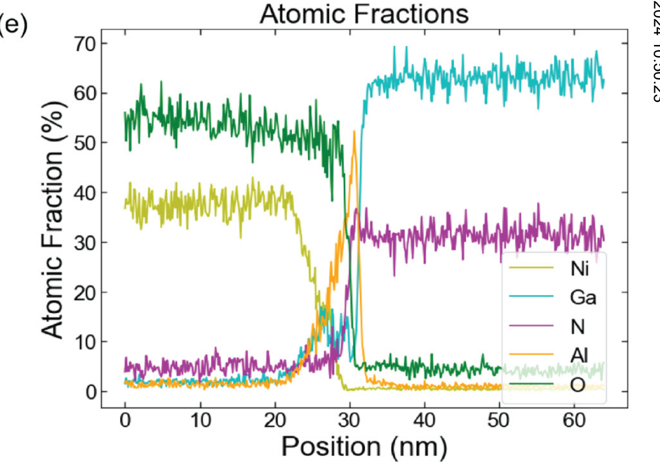


FIG. 2. (a) Low-magnification HAADF-STEM image showing a film stack with protective Pt caps on top that were deposited *in situ* in the FIB. (b) High-magnification HAADF-STEM image from the box in (a) showing a GaN cap, $Al_{0.25}Ga_{0.75}N$ layer, and GaN channel. The interfaces are atomically abrupt with no extended defects observed. The zone axis observed here is [21$\bar{3}$0] with respect to the GaN crystal structure. (c) Vesta model of the GaN structure for the [21$\bar{3}$0] zone axis. (d) Lower-magnification HAADF-STEM image in the nearby region where EDS acquisition was performed also showed damage at the NiO/GaN cap interface. (e) EDS line profile of atomic fractions over the red arrow in (d).

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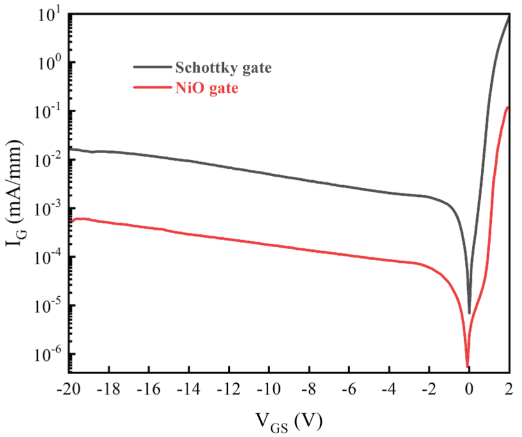
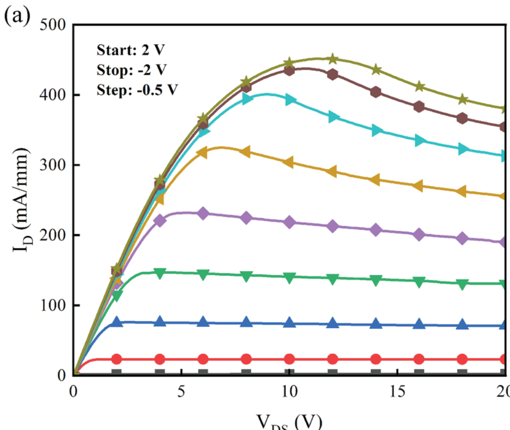


FIG. 3. Gate I–V characteristics from Schottky- and NiO-gated devices.



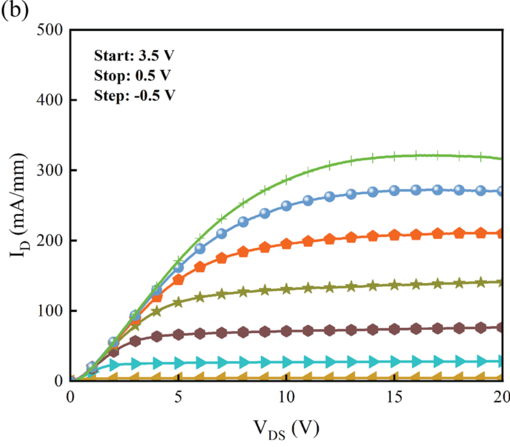


FIG. 4. Drain I–V from (a) Schottky-gated and (b) NiO-gated devices. For the former, the gate voltage is stepped from +2.0 to −2.0 V in steps of −0.5 V, while in the latter, the gate voltage is stepped from 3.5 to 0.5 V in steps of −0.5 V.

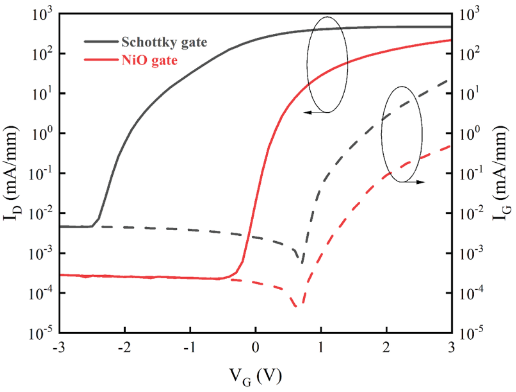


FIG. 5. Drain current-gate voltage characteristics from both types of devices.

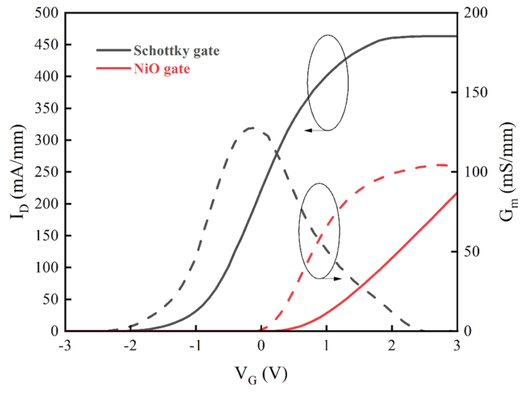


FIG. 6. Transfer characteristics from both types of devices.

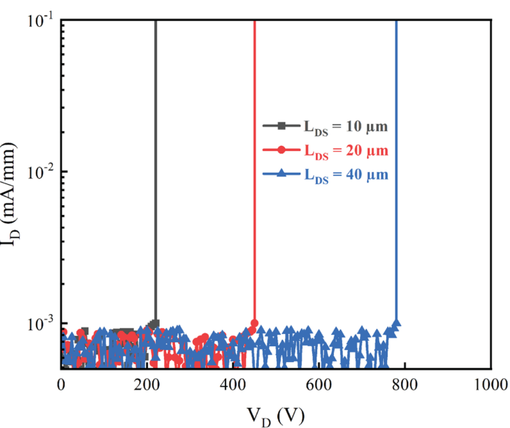


FIG. 7. Breakdown voltage as a function of drain-source distance for NiO-gated HEMTs.

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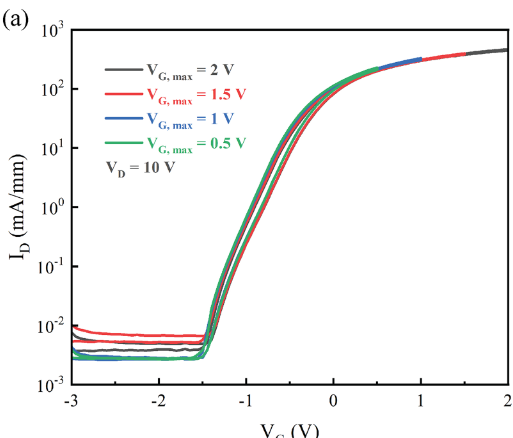
TABLE I. Comparison of the dc performance of reported NiO-gated E-mode HEMTs.

Reference	NiO thickness	NiO doping	Passivation		Gate recess	NiO annealing	Sat. I_d	Resistance	Max G_m	V_{th}
Unit	nm	cm^{-3}		nm	nm		mA/mm	Ohm mm	mS/mm	V
This work	20	10^{18}	No passivation		0	No annealing	300	25	105	0.9
Guo *et al.*[7]	100	2×10^{17}	SiNx	100	9	450 °C Air 10 min	520	11.8	145	1.73
Guo *et al.*[1]	100	1.33×10^{18}	SiNx	200	9	450 °C O_2 10 min	520	10.8	116	0.6
Huang *et al.*[8]	70	10^{18}	AlO	—	0	500 °C O_2 30 min	100	—	55	0.33
Du *et al.*[2]	—	6.0×10^{18}	SiNx	5	0	350 °C N_2 3 min	240	20	40	0.55
Li *et al.*[9]	—	3.8×10^{17}	No passivation		10	400 °C O_2 10 min	170	25	90	0.4

The gate I–V characteristics from the Schottky- and NiO-gated HEMTs are shown in Fig. 3. Note that there is more than one order of magnitude reduction in reverse leakage current due to the larger effective barrier height of the heterojunction gate. The leakage current at −20 V for the Schottky gate was 1.6×10^{-2} mA/mm, while this number decreased to 5.2×10^{-4} mA/mm for the NiO gate. The Schottky barrier height for the former was 0.58 eV with an effective ideality factor of 3.75, indicating the presence of multiple current transport mechanisms.[1,2] The ideality factor for the NiO gate was 2.78.

The I_D–V_{DS} characteristics from the Schottky- and NiO-gated devices are shown in Fig. 4, with excellent saturation performance and maximum saturation output current densities of 450 and 320 mA/mm, respectively. Figure 5 shows the ON/OFF drain current ratios of ~10^5 for Schottky-gated devices and ~10^6 for NiO-gated devices, with subthreshold swings (SS) of 181 and 128 mV/dec, respectively. The on-resistance (*R*on) of 25.2 Ω mm corresponds to a specific on-resistance of (*R*on, sp) of 7.06 mΩ cm^2. The threshold voltages calculated from Fig. 6 were −0.95 V for the Schottky-gated HEMTs, corresponding to depletion-mode operation, while the NiO-gated HEMTs had V_{th} of +0.9 V, corresponding to enhancement mode operation. The maximum transconductance of the NiO-gated devices was 105 mS/mm. The relatively low SS values and good transconductance demonstrate that the p-NiO gate



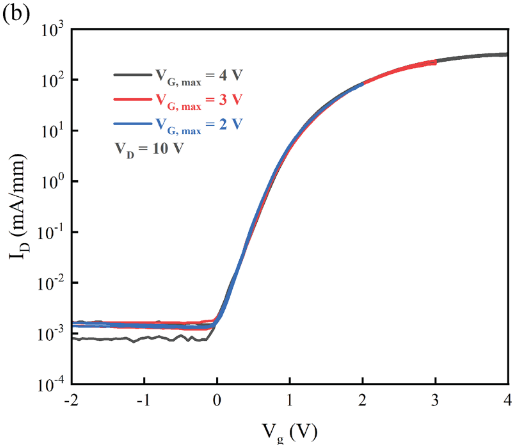


FIG. 8. Pulse-mode transfer curves of (a) Schottky- and (b) NiO-gated devices with various maximum gate voltage sweeps.

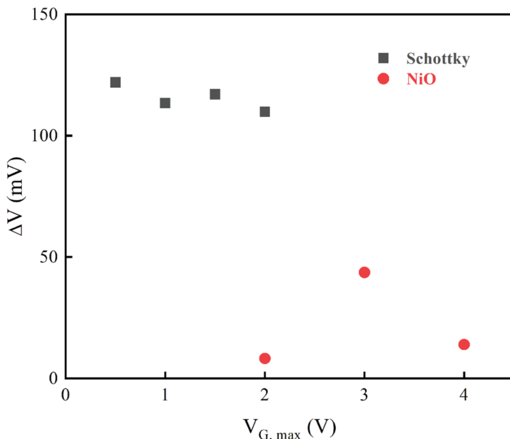


FIG. 9. Gate voltage difference between up sweep and down sweep at a fixed drain current of 1 mA/mm.

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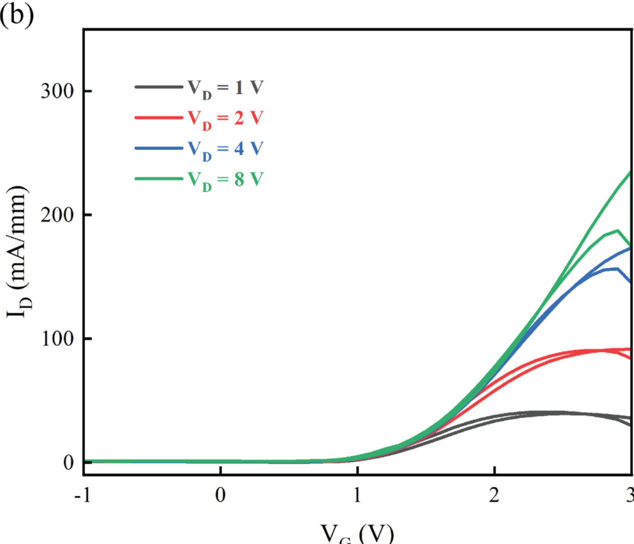

FIG. 10. Pulse-mode transfer curves of (a) Schottky- and (b) NiO-gated devices at various drain voltages.

provides competitive pinch-off characteristics and is a promising option as a p-type gate for GaN-based HEMTs.

The dependence of breakdown voltage, defined as the voltage at a reverse current density of 0.1 mA mm, as a function of drain-source distance is shown in Fig. 7. The values were 220 V for 10 μm, 450 V for 20 μm, and 780 V for 40 μm separation. These correspond to Baliga figures of merit of 6.9, 28.7, and 86.2 MW/cm^2. Table I summarizes a comparison of literature values for NiO-gated HEMTs. What is noteworthy in our case is the absence of any annealing steps or the passivation layer, which still results in decent performance with a simplified fabrication process.

To examine the gate lag effect of both types of devices, the pulse-mode I–V tests were conducted by changing the maximum gate voltage ($V_{g,\ max}$) and the drain voltage. When testing in pulse mode with different $V_{g,\ max}$, the base stress voltage was set at −6 V with a fixed drain voltage of 10 V for both types of HEMTs. The pulse width and period were set to 1 and 20 ms, respectively. For the Schottky-gated devices, the gate voltage rises to the $V_{g,\ max}$ values of 0.5, 1, 1.5, and 2 V in the upward sweep. For the NiO-gated devices, the gate voltage rises to the $V_{g,\ max}$ values of 2, 3, and 4 V in an upward sweep. In the downward sweep, the base voltage was set to the corresponding $V_{g,\ max}$, reducing to −7 V, as depicted in Fig. 8. Both types of devices showed reliable stability under these varying $V_{g,\ max}$ conditions, with no significant divergence. The voltage hysteresis at a drain current of 1 mA/mm was roughly 120 mV for the Schottky-gated devices and below 50 mV for all the NiO-gated devices, as seen in Fig. 9.

For the pulse-mode I–V with various drain voltages, the pulsed gate voltage was swept from −2 to 2 V (Schottky gated) and −1 to 3 V (NiO gated) with the same base stress voltage of −6 V. The drain voltage was varied from 1 to 4 V for the Schottky-gated devices and from 1 to 8 V for the NiO-gated devices. In the descending sweep, the base stress voltage was set at the maximum gate voltage, 2 and 3 V, respectively. The pulsed gate voltage then dropped from this base level to the start of the curves, as illustrated in Fig. 10. These tests showed that the tested drain voltage had a minimal impact on the threshold voltage of both devices. However, it did increase electron trapping in the channel. Notably, both types of devices exhibited minor hysteresis and current variation, but their stability remained satisfactory.

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IV. SUMMARY AND CONCLUSIONS

We describe a simple fabrication process for NiO-gated AlGaN/GaN HEMTs, which provides excellent pinch-off and breakdown characteristics without the need for postNiO deposition annealing or the patterning and deposition of any passivation layers. The other advantages over p-GaN gates include the absence of etching steps or Mg diffusion issues.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

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Author Contributions

Chao-Ching Chiang: Data curation (equal); Formal analysis (equal); Investigation (equal); Writing – original draft (equal). **Hsiao-Hsuan Wan:** Investigation (equal). **Jian-Sian Li:** Investigation (equal). **Fan Ren:** Conceptualization (equal); Project administration (equal); Supervision (equal); Writing – review & editing (equal). **Timothy Jinsoo Yoo:** Formal analysis (equal); Investigation (equal); Writing – original draft (equal). **Honggyu Kim:** Supervision (equal). **S. J. Pearton:** Project administration (equal); Supervision (equal); Writing – original draft (equal); Writing – review & editing (equal).

DATA AVAILABILITY

The data that support the findings of this study are available within the article.

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