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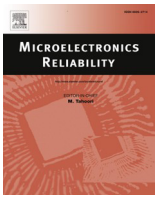

Research Paper

Synergistic effects of heating and biasing of AlGaN/GaN high electron mobility transistors: An in-situ transmission electron microscopy study

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ABSTRACT

High temperature adversely affects the reliability of AlGaN/GaN high electron mobility transistors (HEMTs). Degradation studies typically involve post-mortem visualization of the device cross-section to identify failure mechanisms. In this study, we present an in-situ technique by operating the transistor inside the transmission electron microscope (TEM) for real time observation of the defects and failure. A custom-made MEMS chip facilitates the simultaneous biasing and heating capability inside the TEM. The results indicate that the high temperature operation promotes nucleation of new defects in addition to the propagation of existing defects, which degrade the performance of the device even at low biasing conditions. The gate Schottky contact is found to be the most vulnerable region at elevated temperature. The diffusion of gate metals, especially the diffusion of Au at the metal-semiconductor interface initiates the gate degradation process, as confirmed by energy dispersive X-ray spectroscopy (EDS), followed by catastrophic failure with the increase of operation temperature and drain biasing voltage. The high-resolution TEM imaging along with geometric phase analysis reveals the evolution of defect clusters, such as dislocations networks, stacking faults, and amorphized regions, in the AlGaN and GaN layers, which increases the lattice strain leading to catastrophic failure at elevated temperature. The insights obtained from the in-situ study may be useful in improving high temperature HEMT reliability.

1. Introduction

AlGaN/GaN high electron mobility transistors (HEMTs) are well-suited for high power, high frequency, high speed, and high temperature applications [1–16]. The wide bandgap AlGaN/GaN heterostructure provides high breakdown voltage, good thermal stability, and high radiation tolerance [17,18]. They also exploit the advantage of high electron concentration at the AlGaN/GaN interface, known as two-dimensional electron gas (2DEG), that develops due to piezoelectric and spontaneous polarization effects. The high electron mobility and saturation velocity of 2DEG yield a higher power output density and lower on-resistance. However, these devices are yet to meet the predicted performance and reliability [19,20]. The high-power density of GaN HEMTs is always accompanied by high thermal stress due to self-heating of the device despite having good thermal conductivity of the materials [21–23]. Additionally, the high electric field induced inverse piezoelectric stress also deteriorates the device reliability during high voltage operation [19,23,24]. The device reliability is further compromised in high temperature environment due to the development of additional thermal stress among the dissimilar epitaxial layers of mismatched thermal expansion coefficients and lattice constants [25–27].

The failure mechanisms of HEMTs are complex and multifaceted, typically stemming from a combination of material defects, device design, and operational stressors. Material defects such as dislocations, cracks, and impurities within the GaN and AlGaN layers can act as nucleation sites for structural degradation under high electrical fields and temperatures. The electrically active defects can capture and emit carriers generating trap. The traps near the 2DEG can be ionized by

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capturing electrons, and these negatively charged traps create depletion region in 2DEG by reducing electron density. This causes a delay of conduction state by increasing the dynamic ON-resistance when the gate is switched ON, which results in transient drain current known as current collapse or gate lag effect [28]. The harsh operating conditions such as radiation further reduces the reliability of GaN HEMTs through ionization and displacement damage, which may result in single event effect or permanent device failure [18,29]. The radiation induced defects in GaN HEMTs can cause threshold voltage shift, mobility and transconductance reduction, increase of gate leakage and noise. Additionally, the lattice mismatch between GaN and AlGaN layers can introduce strain, leading to mechanical stress and subsequent device failure. Device design attributes, such as inadequate gate dielectric integrity or poor thermal management, can exacerbate these issues by facilitating the onset of breakdown mechanisms such as gate leakage or thermal runaway. The gate failure of GaN HEMTs is attributed to inverse piezoelectric field effect, temperature, electrochemical reaction, dislocations, and thermal expansion mismatch of gate metal stack and AlGaN barrier [27]. Operational stressors, including high voltage or current densities, can accelerate degradation processes such as electron trapping, leading to reduced device performance and eventual failure. The short circuit and electrostatic discharge (ESD) failures are other reliability concerns of GaN HEMTs for high voltage and high current applications, which are attributed to hotspot and filament formation, gate-source diode breakdown, poor MESA definition, and high contact resistivity [30,31]. Understanding and mitigating these failure mechanisms are crucial for improving the reliability and longevity of GaN/AlGaN HEMTs in various electronic applications.

Extensive research on post-failure analysis of AlGaN/GaN HEMTs has been conducted in the literature as part of the effort to enhance reliability by employing Raman spectroscopy, X-ray diffraction techniques, cathodoluminescence, optical and scanning electron microscopy (SEM), and transmission electron microscopy (TEM) [19,24,32–40]. TEM provides excellent through-thickness visualization with atomic scale resolution accompanied by other analytical capabilities such as electron diffraction, electron energy loss spectroscopy (EELS), and energy dispersive X-ray spectroscopy (EDS). As a result, TEM is extensively used in analysis of GaN HEMTs to identify the defects, failure locations, and failure mechanism [37,41–45]. However, traditional TEM characterization of electronic devices requires tremendous efforts to connect the post-experiment visual information to the electrical properties of the bulk device due to scaling factors and often fails to provide fundamental information on the nucleation and evolution of defects [46]. Therefore, in recent years, in-situ TEM study has gained a lot of attraction due to the advantage of real-time visualization instead of post-experiment visualization, where intermittent information at the nanoscale is often missed. However, in-situ TEM characterization of the AlGaN/GaN HEMTs remains challenging due to meticulous requirement of in-situ device preparation with proper electrical connections for biasing preserving the epitaxial integrity of the of device.

Only a handful of research demonstrated the in-situ operation and characterization of AlGaN/GaN HEMTs inside the TEM [47–50]. Wang et al. [47] demonstrated the in-situ failure mechanism of AlGaN/GaN HEMT at ON condition where the failure was driven by self-heating of the device. Islam et al. [48,49] demonstrated the in-situ operation of AlGaN/GaN HEMTs at OFF conditions, where pre-existing lattice defects significantly impact the device failure mechanism. However, all these existing efforts are focused on biasing effects. Since these devices are touted for extreme environment applications, both externally applied temperature and biasing should be a more suitable investigation. The motivation for this study comes from the lack of in-situ TEM studies in the literature that have examined the impact of external heating during biasing of AlGaN/GaN HEMTs.

In this study, we demonstrate the simultaneous effect of heating and biasing of AlGaN/GaN HEMT inside the TEM. A custom-built micro-electro-mechanical system (MEMS) chip facilitated the feasibility of conducting such a study, allowing for biasing of the device inside the TEM while simultaneously generating heat. The motivation of this study arises from the high temperature reliability issue of AlGaN/GaN HEMT [27,36,43] and to pinpoint the vulnerable location of the device when operating at elevated temperature. Multiple studies in literature reported the electrical stress induced degradation of bulk GaN HEMTs after hundreds of hours of operation at elevated temperature [27,34,43]. The potential benefits of in-situ TEM are to accelerate the reliability study due to examination of a thin lamella of device instead of bulk device, while providing precise insight of degradation and failure mechanism at the atomic scale resolution. The demonstration of this in-situ biasing and heating of AlGaN/GaN HEMTs can be extended to study the reliability of other electronic devices.

2. Experimental

The in-situ TEM investigation of simultaneous effect of heating and biasing in AlGaN/GaN HEMTs was performed using a custom designed MEMS chip. The built-in heating coil of the MEMS chip accommodates both heating and biasing options simultaneously. The MEMS chip was fabricated on silicon-on-insulator (SOI) substrate using conventional nanofabrication technique. The commercially available SOI wafers had 20 μm of device layer, 450 μm of handle layer, and 2 μm of buried oxide (BOX) layer. The steps of nanofabrication involved photolithography of device features, deep reactive ion etching (DRIE) to etch through the device layer, backside alignment and photolithography of backside patterns that defined the perimeter of the chips, DRIE to etch through the handle layer followed by wet etching of BOX layer using buffer oxide etchant (BOE). The fabrication details of the MEMS chip can be found elsewhere [51]. The SEM image of the fabricated MEMS chip is shown in Fig. 1a. The chip was operated under the infrared thermal microscope (Optris PI-640) to determine the temperature of the heating coil with respect to the applied voltage. A thermal microscopic image of the MEMS chip is provided in Fig. 1c showing the temperature rise of the heater to 235 °C at 6 V of applied voltage across the heating pads in ambient condition. The actual temperature during in-situ operation is significantly higher inside the TEM due to reduced heat dissipation under vacuum.

Commercially available depletion mode normally-ON bare die of AlGaN/GaN HEMT on SiC substrate (Wolfspeed®, CGHV60008D), shown in Fig. 1d, was used. The SEM cross-sectional image of the device is shown in Fig. 1e. For in-situ TEM experiment, approximately 3 μm thin lamella of AlGaN/GaN HEMT was prepared from the bare die after depositing protective carbon layer on top of the insulated SiN_x passivation layer of the device using FEI Scios-2 DualBeam FIB system equipped with gallium ion (Ga^+) source. The lamella was transferred into the heater of the MEMS chip using FIB in-situ manipulator needle as shown in Fig. 1 f-g. The drain and source electrodes of the thin device were connected to the heater electrode using carbon deposited pads (Fig. 1 h). The top protective carbon layer was cut off to prevent leakage of current through the carbon layer during biasing. Finally, the 3 μm thin lamella of GaN HEMT was thinned down to ~200 nm using FIB voltage of 30 to 2 kV and probe current of 1 nA to 78 pA to make it electron transparent (Fig. 1i). The MEMS chip along with the thinned GaN HEMT was mounted on Aduro (Protochips®) biasing and heating holder. A schematic structure of the HEMT is shown in Fig. 1j for better illustration.

A FEI Talos F200X S/TEM system equipped with EDS detector was used for the in-situ biasing and heating experiment. The in-situ biasing was performed at zero gate voltage ($V_{gs} = 0$ V) and drain voltage (V_{ds}) of 2 V, 4 V, 6 V, and 7 V. The device was held at each simultaneous biasing and heating condition for 1 min before proceeding to the subsequent step. The bright field TEM images and EDS data were acquired after each biasing and heating step.

Additionally, ex-situ die-level electrical characterization of the GaN HEMTs was performed at elevated temperature ranging from room

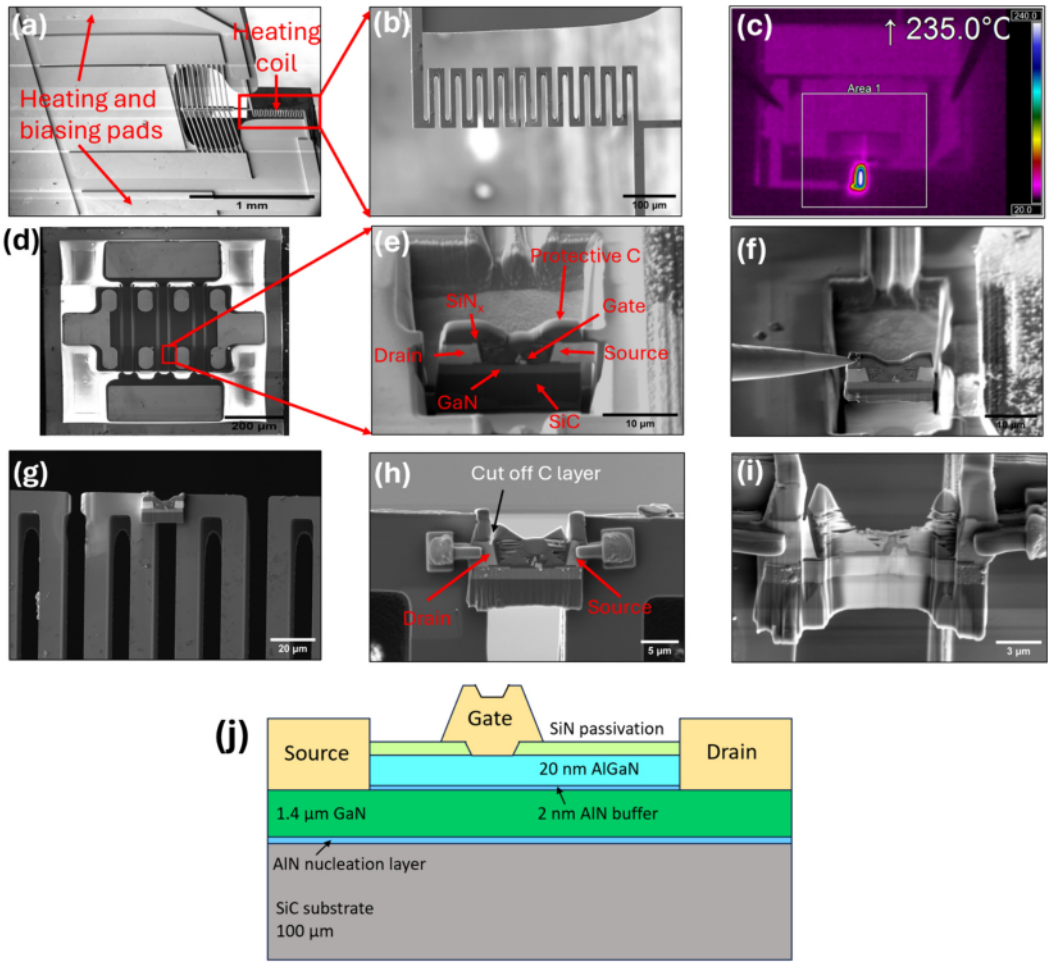

Fig. 1. (a-b) SEM image of the heating and biasing MEMS chip, (c) thermal microscopic image of the device showing the temperature of the heater at 6 V, (d) SEM image of the bulk GaN HEMT, (e) cross-section of the HEMT, (f) lift-out of thin section of the HEMT, (g) installation of the HEMT lamella into the MEMS chip heater, (h) forming source and drain connections after transferring the lamella into the heater, (i) final thinning of the lamella, (j) schematic structure of the HEMT.

temperature to 300 °C in Cascade FormFactor 11000 probe station equipped with thermal stage ranging from −60 to 300 °C.

3. Results and discussion

The die-level DC characteristics of the bulk AlGaN/GaN HEMT at elevated temperature are shown in Fig. 2a-c. The performance of the device degrades with the increase of operating temperature from ambient condition to 300 °C. The output curve (Fig. 2a) reveals the decrease of drain current along with increase of ON-resistance of the device with the increase of temperature. The transfer curve (Fig. 2b) shows a negative shift of threshold voltage from −2.90 V at room temperature to −3.05 V at 300 °C. The reduced drain current with respect to the gate voltage of the device indicates reduction of transconductance with the increase of temperature. The degraded output current and transconductance of the device could be attributed to the reduction of carrier mobility due to polar optical phonon scattering [52,53] and/or generation of defects in the epitaxial layers of the device due to thermal stress developed inside the device, which may act as carrier trap centers [54,55]. Approximately a 2 order of magnitude higher leakage current is also monitored (Fig. 2c) when the operating temperature of the device is increased from room temperature to 300 °C. The negative shift of the threshold voltage and higher leakage current suggest degradation of gate contact and diffusion of gate metals at the interface [27,43].

The representative equivalent circuit of the GaN HEMT on the MEMS heating chip is shown in Fig. 2d. The in-situ IV characteristics of the heating chip, with and without the thin lamella of GaN HEMT mounted on it, are presented in Fig. 2e. The black and red curves illustrate the IV characteristics for the heater with and without the GaN HEMT, respectively. In the absence of the GaN HEMT, the heating chip is essentially a resistor. The output curve of the thin lamella of GaN HEMT was obtained by subtracting the current output of the heating chip without HEMT from that of the heating chip with the HEMT. The extracted output current density of AlGaN/GaN HEMT lamella during the in-situ TEM experiment is shown in Fig. 2f. The in-situ output characteristics of the GaN HEMT indicate that the drain current at zero gate voltage saturates at approximately 3.5 V of drain voltage, where it reaches a peak current density of 3.1 A/mm. However, the drain current deteriorates beyond 3.5 V due to the evolution of higher external temperature and self-heating at higher biasing voltage.

To determine the heater temperature due to Joule heating during in-situ biasing, multi-physics simulation was performed using Ansys software. The simulation was performed on the actual MEMS geometry under vacuum to mimic the TEM chamber. The temperature field of the heater at different biasing voltage is shown in Fig. 3. The maximum temperature is obtained at the middle section of the heater, where the thin GaN HEMT TEM lamella is mounted. The maximum temperature at 2, 4, 6, and 7 V is found to be 83, 298, 542, and 684 °C, respectively.

The low magnification bright field TEM images of the GaN HEMT at 0, 2, 4, 6, and 7 V of drain bias (V_{ds}) are shown in Fig. 4a-e. In pristine condition (V_{ds} = 0 V, 22 °C) (Fig. 4a), multiple defects within the GaN buffer layer, primarily located at the GaN/SiC substrate interface

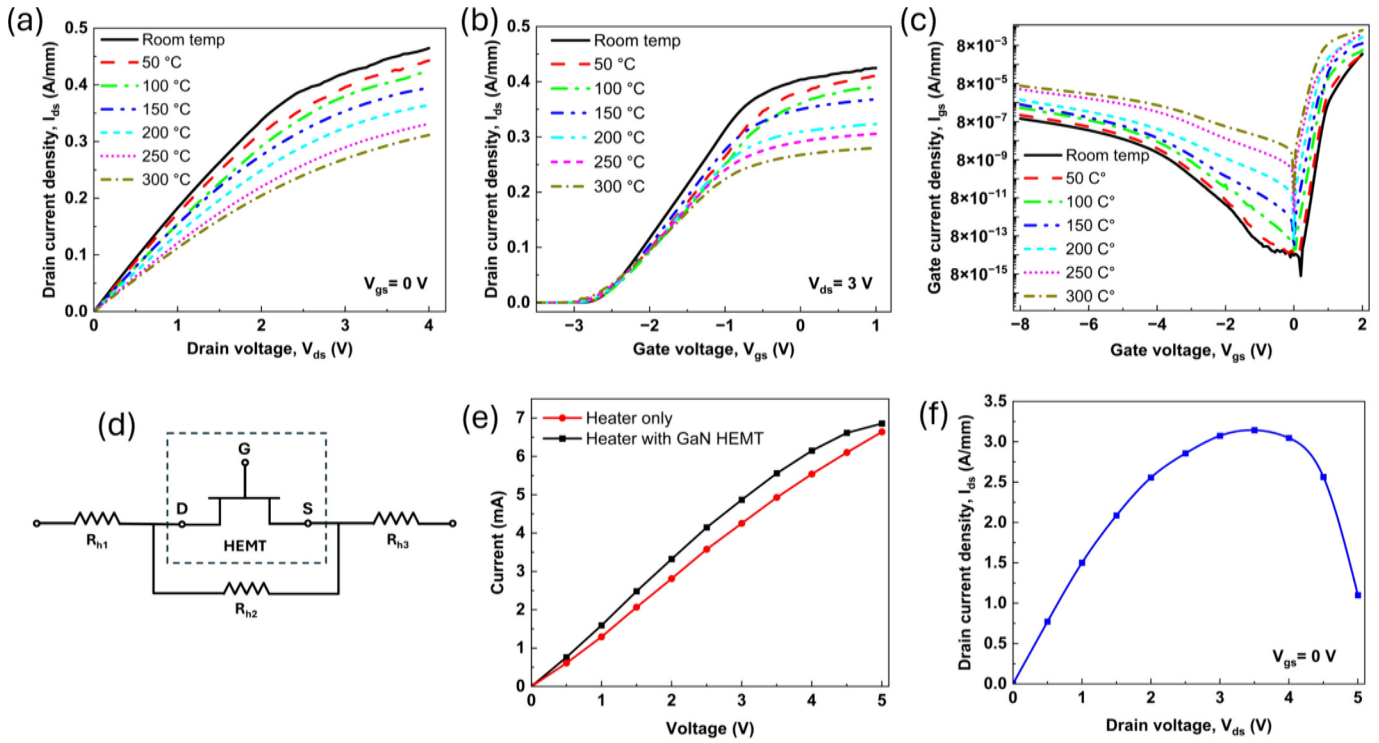

Fig. 2. (a-c) Die-level DC characterization of AlGaN/GaN HEMT, (a) output curve at V_{gs} = 0 V, (b) transfer curve at V_{ds} = 3 V, (c) gate leakage. (d) representative equivalent circuit of HEMT and heater (R_h represents the heater resistance), (e) in-situ IV characterization of AlGaN/GaN HEMT with and without heater, (f) drain current density of the HEMT during in-situ experiment.

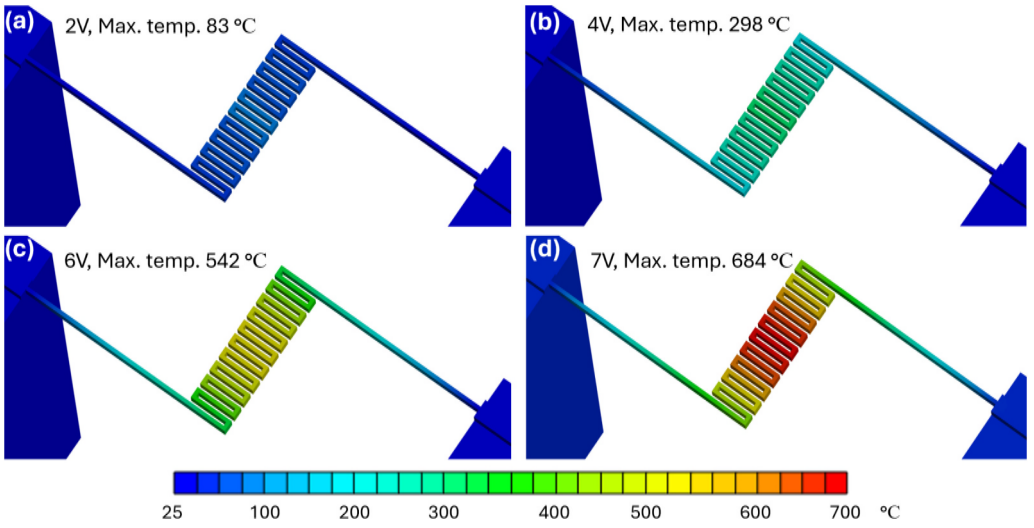

Fig. 3. Ansys multi-physics simulation of temperature field of the heater at (a) 2 V, (b) 4 V, (c) 6 V, and (d) 7 V. The model was calibrated with experimental results after including up natural convective heat transfer.

(highlighted by yellow arrowheads), are observed. These defects likely originated during fabrication due to the mismatch of lattice constants and thermal expansion coefficients among the heteroepitaxial layers [56–58]. As the biasing voltage and device heating temperature increase, pre-existing defects extend deeper into the GaN buffer layer, accompanied by the generation of new defects, as shown by the yellow and blue arrowheads, respectively, in Fig. 4b-d. In addition to crystallographic defects in the epitaxial layers, gate failure of the device occurs at 6 V of drain voltage (Fig. 4d) with a simultaneous heating temperature of 542 °C. The damage of the field plate is also monitored at this biasing and heating condition. The initiation of gate failure predominantly occurs at the drain side of the gate edge (indicated by red arrowhead), a known vulnerable spot in GaN HEMTs due to high electric field-induced inverse piezoelectric stress [19,32,36].

In the high electric field region of AlGaN/GaN HEMTs, several specific degradation mechanisms can occur, leading to device failure. One prominent mechanism is impact ionization, where high electric fields cause electron-hole pairs to generate carriers via impact ionization, leading to avalanche breakdown. This phenomenon can induce hot carrier effects, such as electron trapping in the gate dielectric or interface states, ultimately degrading device performance. Another degradation mechanism is electron trapping in the AlGaN barrier layer,

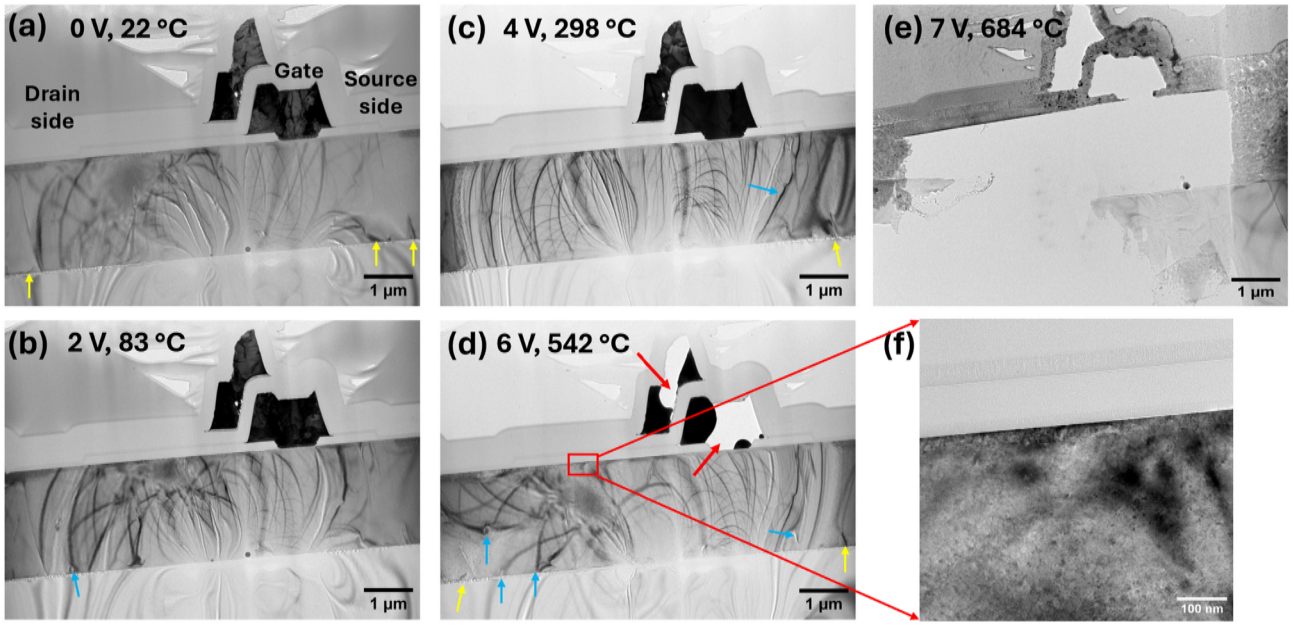

Fig. 4. Low magnification bright field TEM images at different biasing and heating conditions. (a) no biasing and at room temperature, (b) V_{ds} = 2 V at 83 °C, (c) V_{ds} = 4 V at 298 °C, (d) V_{ds} = 6 V at 542 °C, (e) V_{ds} = 7 V at 684 °C, and (f) magnified image of drain access region after biasing at V_{ds} = 6 V at 684 °C.

caused by defects such as threading dislocations and point defects. These trapped electrons can affect the device's threshold voltage and increase leakage current, leading to reduced reliability. Furthermore, traps at the AlGaN/GaN interface can result in charge trapping and detrapping, causing threshold voltage instability and hysteresis in device characteristics. In addition, thermal effects in the high field region can exacerbate degradation, including self-heating due to high power dissipation and thermal-mechanical stress-induced degradation of the material properties. Additionally, the diffusion of gate metals in the presence of elevated temperature could lead to accelerated failure of the gate contact. Upon increase of the biasing condition to 7 V with simultaneous temperature of 684 °C, catastrophic failure of the entire device is observed, as shown in Fig. 4e. Previous in-situ TEM biasing studies of AlGaN/GaN HEMTs by Islam et al. [48,49] reported that the catastrophic failure occurs above 20 V when the device is operated in OFF state. The early breakdown of the device here in ON state is the result of uncontrolled generation of defects within the device due to combined effect of high electric field from biasing and thermal field coming from both self-heating of the device itself due to very high current density and external heating by the MEMS chip. The severity of degradation of epitaxial layers of the device could be observed in Fig. 4f during biasing the device at 6 V and 542 °C. It is important to note that the temperature values reported in this manuscript are due to external heating of the device, which are determined by Ansys simulation as mentioned earlier. The actual device temperature could be higher due to self-heating as a result of biasing.

The essence of this in-situ experiment is the demonstration of the failure mechanism with pinpointing the vulnerable spots during operation when the GaN HEMT is under synergistic effects of electric and thermal field, rather than determining absolute values of the breakdown voltage and temperature of the device, which would be unrealistic due to scaling factor involved in comparing a ~ 200 nm thin lamella of GaN HEMT with bulk device. In these passivated devices we did not observe electrolytic-enhanced degradation, which involves the interaction of moisture or contaminants with the device under bias conditions, leading to accelerated degradation. This mechanism typically occurs when the HEMT is subjected to high electric fields and temperatures, creating conditions conducive to electrochemical reactions at the device's surface. Moisture or contaminants present on the surface can ionize under the applied electric field, forming an electrolyte layer. This electrolyte layer can facilitate the migration of ions and charge carriers, leading to electrochemical reactions such as oxidation or reduction at the metal-semiconductor interface or within the device's layers. The electrolytic-enhanced degradation mechanism can manifest in several ways. For example, at the gate electrode interface, moisture or contaminants can lead to the formation of a conductive oxide layer, affecting the gate control and increasing leakage currents. Additionally, electrolytic corrosion of the metal contacts can occur, leading to increased contact resistance and degraded device performance. Furthermore, if the electrolyte layer penetrates the device's layers, it can induce metal migration, causing short circuits or altered electrical properties.

To monitor the evolution of defects during operation with temperature, the high magnification TEM images near the gate area of the device under different biasing conditions are shown in Fig. 5a-h. Couple of defect clusters, mainly dislocations are observed at the AlGaN/GaN interface and the GaN buffer layer in the source to gate access region of the pristine device (Fig. 5a). The subsequent increase of biasing voltage and temperature, the pre-existing defect at the AlGaN/GaN interface continues to grow larger with additional defect degeneration in the surrounding area (Fig. 5c and e). At 6 V, the dislocation network extends throughout the GaN buffer layer (Fig. 5g), which acts as the breaking line at 7 V and 684 °C, as shown in Fig. 4e. In the drain to gate access region, the cluster of defects, mostly vacancy clusters and amorphization, are observed in the AlGaN layer at 4 V, as indicated by the yellow box in Fig. 5f. At 6 V of drain bias, the cluster of defects spread throughout AlGaN layer towards the drain (indicated by yellow box in Fig. 5h) accompanied by additional dislocation network in the GaN buffer layer (yellow arrowhead in Fig. 5h). The initiation of gate metal damage is observed to commence at 4 V and 298 °C, as highlighted by the blue arrowhead in Fig. 5e and f. The gate contact stability of GaN HEMTs has been reported to be approximately 400 °C [36,59]. The early onset of gate degradation here could be due to high current density of the thin TEM lamella during biasing.

Crystallographic defects under the gate area prior to gate failure can potentially lead to reduced output current, higher leakage current, and threshold voltage shift in GaN HEMTs. To visualize the crystal defects generated during biasing at elevated temperature, high resolution TEM imaging was acquired under the gate, as shown in Fig. 6. The atomic

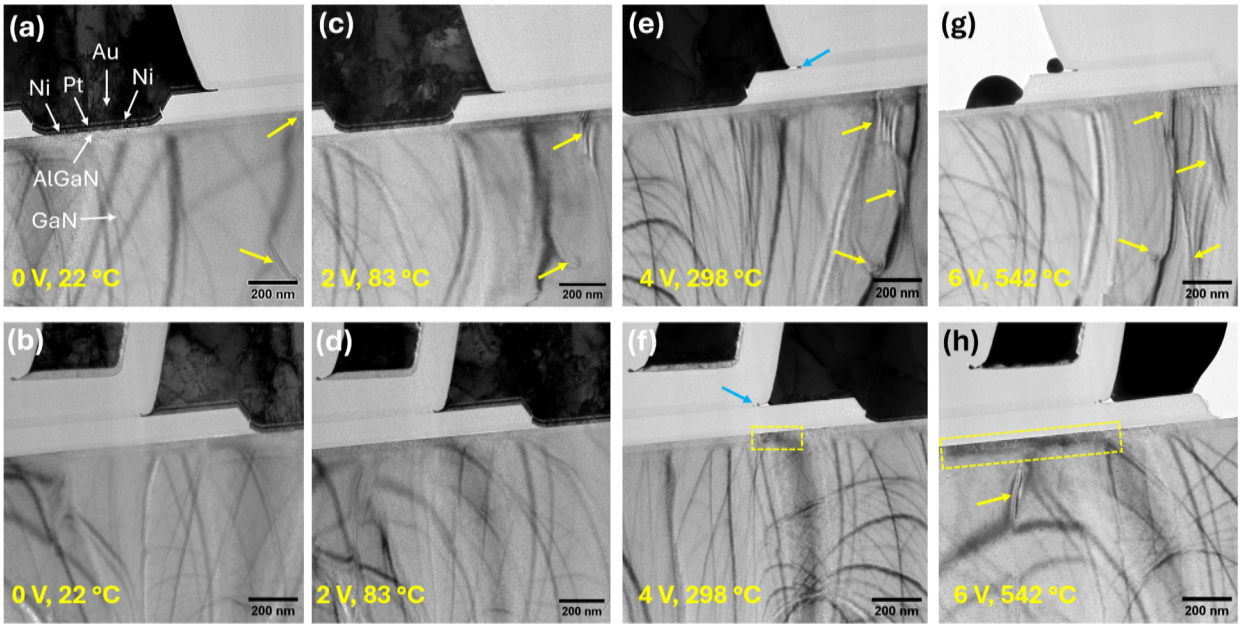

Fig. 5. Magnified bright field TEM images near the gate area at different biasing and heating conditions. (a) source and (b) drain side of pristine device at room temperature, (c) source and (d) drain side at V_{ds} = 2 V and 83 °C, (e) source and (f) drain side at V_{ds} = 4 V and 298 °C, (g) source and (h) drain side at V_{ds} = 6 V and 542 °C.

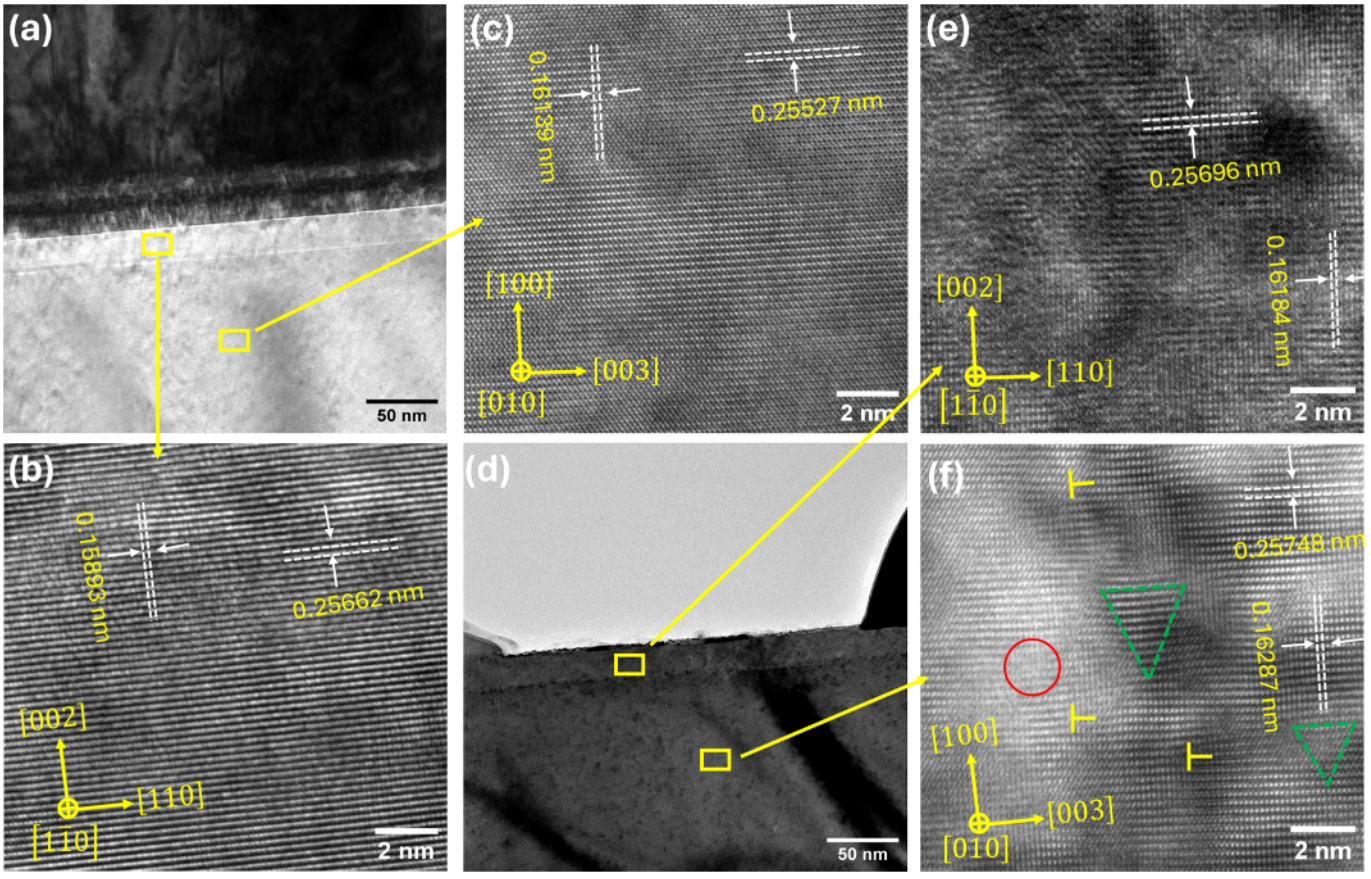

Fig. 6. High resolution TEM images. (a) under the gate region, (b) AlGaN layer, and (c) GaN layer of pristine HEMT. (d) under the gate region, (e) AlGaN layer and (f) GaN layer after biasing at 6 V at 542 °C.

resolution TEM images of AlGaN and GaN layer of the pristine device are shown in Fig. 6b and Fig. 6c, respectively. Both AlGaN and GaN layer demonstrate good crystal quality with minimal defects. A large number of defects are observed in the AlGaN and GaN layer after biasing at elevated temperature. Fig. 6e and Fig. 6f show the atomic resolution images of the AlGaN and GaN layers, respectively, after biasing at 6 V

and 542 °C. The d-spacing values of the two perpendicular lattice planes of AlGaN and GaN layers have been reported in Table 1. The d-spacing values of both AlGaN and GaN layers are found to increase after biasing the device at 6 V and 542 °C. The d-spacing values are calculated at room temperature to eliminate the thermal expansion effect during heating. The increase of d-spacing of the lattice planes indicates the increase of lattice strain. Additionally, widespread amorphized regions and vacancy clusters are observed in the AlGaN layer after biasing at elevated temperature (Fig. 6e). The GaN layer (Fig. 6f) contains multiple screw dislocations (marked by yellow signs), stacking faults (marked by green triangle), and small areas of amorphizations (marked by red circle).

To better illustrate the localized defects, geometric phase analysis (GPA) was performed on the atomic resolution images of the AlGaN and GaN layers obtained on the yellow boxed regions in Fig. 6a and Fig. 6d. The GPA strain maps assist in identifying individual dislocations by revealing localized tensile and compressive strain fields surrounding the dislocation core, stemming from the presence of extra atomic plane. The in-plane (ε_{xx}) and out of plane (ε_{yy}) strain maps of the AlGaN (Fig. 7a and b, respectively) and GaN (Fig. 7c and d, respectively) layer of the pristine device reveal the presence of a small number of dislocations. A significant increase of dislocations is observed after biasing the device at 6 V and 542 °C in both AlGaN (Fig. 7e and f) and GaN (Fig. 7g and h) layers. The proliferation of defects within the AlGaN and GaN buffer layers deteriorates the electrical transport properties of the device during biasing at elevated temperatures, as elucidated in Fig. 2. These nanoscale defects could potentially act as trap centers and scattering centers for electrons reducing the mobility of the device reducing the drain output current and transconductance. Additionally, the high concentration of defects forms conductive percolation paths leading to higher leakage current [37,39].

To examine the gate Schottky contact during biasing at elevated temperature, elemental mapping was recorded by EDS. The elemental chemical mapping of the GaN HEMT in pristine condition (shown in Fig. 8) reveals the presence of stacked metals. The gate metallization consists of the first layer of Ni on top of the AlGaN layer, followed by a thin Pt layer, a second Ni layer, and finally the Au metal. The EDS elemental mapping of the device after biasing at 4 V and 298 °C shows the diffusion of gate metals (Fig. 9). The interdiffusion of Ni and Pt is observed at both Ni/Pt interfaces, whereas direct diffusion of Au metal at the Schottky contact is very prominent. The quantitative comparison of elements obtained by line scanning from Au layer to the GaN layer is shown in Fig. 10. The Ni at the AlGaN/Ni Schottky interface is partially substituted by Au, while most of the Ni at the Au/Ni interface is substituted by Au. The diffusion of Pt at the AlGaN/Ni interface is also observed resulting in lower Pt content at the Pt layer. The sidewalls of the gate could be the dominant diffusion path of Au into the Schottky interface during high temperature operation [27,38,43]. However, no elemental gradient of Au at the Schottky interface is observed along the gate contact. Therefore, we speculate that in addition to sidewall diffusion, partial diffusion of Au can occur through the Pt layer due to the defects created at the Pt layer because of small Pt diffusion during high temperature biasing. The degradation of gate Schottky contact reduces the barrier height of the device increasing the gate leakage current, as observed in die level characterization of the device. In addition to higher leakage current, the intermixing of gate metals also degrades the stability of the gate contact leading to complete failure of the gate at higher voltage and temperature, as seen at 6 V and 542 °C.

The findings of this in-situ TEM study suggest that under high temperature operation the most vulnerable location of the device is the Schottky gate interface, even when no biasing voltage is applied at the gate. This suggests that the observed degradation/failure of the gate is dominated by thermal stress rather than the electric field induced inverse piezoelectric stress when operating the device at elevated temperature. The external heating source along with self-heating of the device due to joule heating contributes to the thermal stress. The degradation of the gate nucleates from the diffusion of gate metals at the interfaces. The mismatch of thermal expansion coefficients of different materials of the gate stacks and the AlGaN/GaN layer accelerates degradation of gate leading to the catastrophic failure of the gate at 542 °C even at zero gate voltage and only 6 V of drain voltage. The thermal un-stability of the Ni/Pt/Au-based Schottky gate contacts has been reported in literature after electrical stressing of the devices for prolonged period [27,36]. The high thermal field also increases the lattice temperature of AlGaN and GaN layers generating vacancies, interstitials, and dislocations. These defects accumulate and interact with each other at high temperature producing stacking faults, vacancy/interstitial clusters, dislocation networks, and extended amorphized regions. These defects increase the lattice strain, which exceeds the elastic limit of the material at some point leading to the catastrophic failure of the device.

Table 1
The d-spacing values of AlGaN and GaN layers of pristine and after biasing at 6 V and 542 °C.

Epilayer	Zone axis	Lattice plane	d-spacing (nm)		Relative change (%)
			Pristine	V_{ds} = 6 V at 542 °C	
AlGaN	$[1\bar{1}0]$	[002]	0.25662	0.25696	0.132
		[110]	0.15893	0.16184	1.830
GaN	[010]	[100]	0.25527	0.25748	0.866
		[003]	0.16139	0.16287	0.917

4. Conclusions

We investigated the synergistic effects of biasing and external heating on the degradation and failure mechanism of AlGaN/GaN HEMTs. Bias can enhance degradation in GaN/AlGaN HEMTs through the creation of high electric fields, exacerbation of electrochemical reactions, and induction of thermal effects, all of which can accelerate device degradation. Instead of conventional post-experiment TEM characterization to identify the nucleation and propagation of defects, we adopted in-situ operation of an electron transparent AlGaN/GaN HEMT inside the TEM using a custom designed heating and biasing MEMS chip. The normally-ON HEMT was operated at different drain bias conditions at elevated temperature ranging from room temperature to 684 °C. The gate Schottky contact emerges as the most vulnerable location during real-time visualization of the device under high-temperature operation. The degradation of the gate contacts nucleates by the interdiffusion of gate metals, especially diffusion of Au at the Ni/AlGaN interface at a temperature as low as 298 °C and 4 V of drain bias. The gate electrode experiences catastrophic failure upon further increase in operating temperature and drain biasing voltage due to mismatch of thermal expansion coefficients of gate and interface materials. The catastrophic failure of the gate in the absence of any gate biasing voltage during high temperature operation reveals the dominant contribution of thermal field due to external heating and device self-heating induced thermoelastic stress over electric field induced inverse piezoelectric stress. The AlGaN and GaN layer nucleates crystal defects along with the propagation of pre-existing defects during high temperature operation. These defects accumulate and react with each other to form defect clusters such as stacking faults, dislocation networks, vacancy/interstitial clusters, and amorphized regions with the increase of operating temperature and biasing voltage leading to increase lattice strain of the epitaxial layers, which ultimately cause catastrophic failure of the device. The results provide valuable insight into the degradation and failure process of AlGaN/GaN HEMT during high temperature operation. It also reflects the importance of proper thermal management to improve reliability of GaN HEMTs in extreme environments. However, additional in-situ experiment is required to better understand the high temperature reliability under different gate biasing conditions both ON and OFF state of

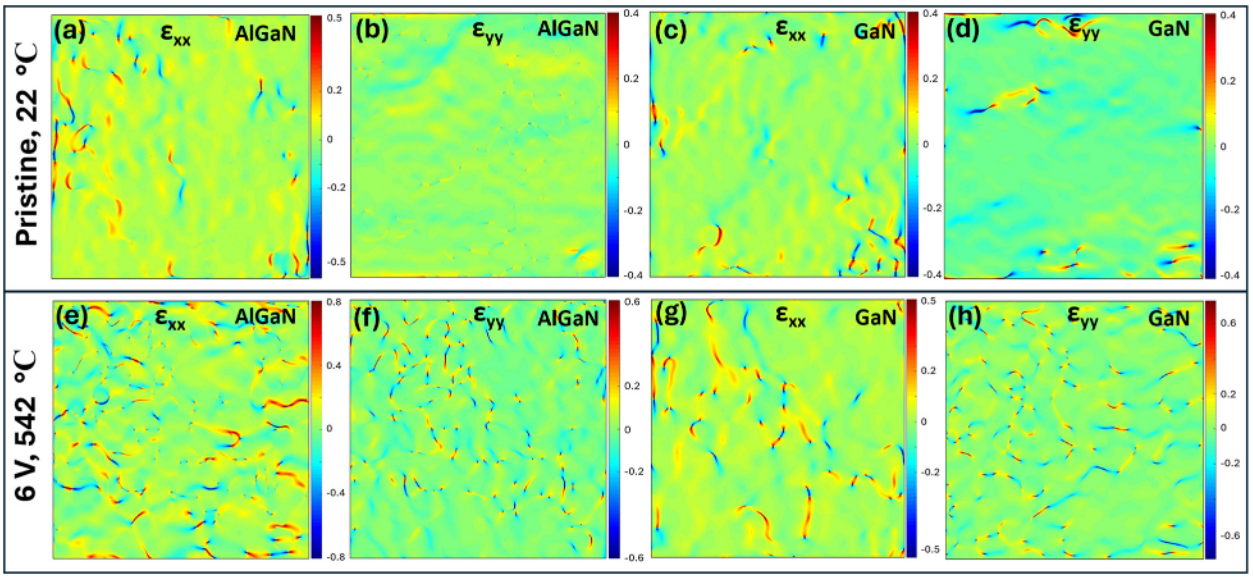

Fig. 7. GPA strain maps. (a-d) pristine condition, (a) ε_{xx} and (b) ε_{yy} of AlGaN, (c) ε_{xx} and (d) ε_{yy} of GaN layers in pristine condition. (e-h) after biasing at 6 V and 542 °C, (e) ε_{xx} and (f) ε_{yy} of AlGaN, (g) ε_{xx} and (h) ε_{yy} of GaN layers at V_{ds} = 6 V and 542 °C. Scale bar shows percentage strain.

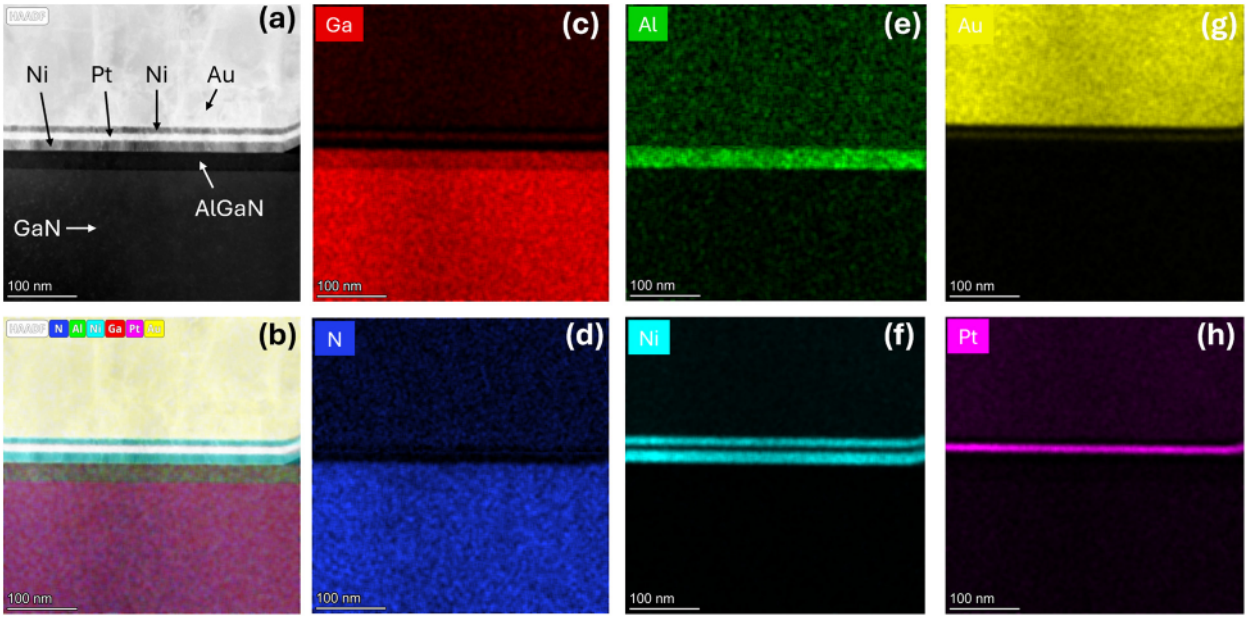

Fig. 8. EDS elemental mapping under the gate region of the pristine device at room temperature. (a) high angle annular dark field (HAADF) image. Elemental EDS maps of (b) all elements, (c) Ga, (d) N, (e) Al, (f) Ni, (g) Au, (h) Pt.

the device. Additionally, degradation of ohmic drain and source contacts during high temperature operation should also be investigated by in-situ experiments to further increase reliability and optimize the design and performance of AlGaN/GaN HEMTs.

CRediT authorship contribution statement

Nahid Sultan Al-Mamun: Conceptualization, Methodology, Validation, Formal analysis, Investigation, Data curation, Writing – original draft. **Ahmad Islam:** Formal analysis, Investigation, Writing – review & editing, Visualization, Funding acquisition. **Nicholas Glavin:** Formal analysis, Investigation, Writing – review & editing, Visualization, Funding acquisition. **Aman Haque:** Conceptualization, Methodology, Validation, Formal analysis, Investigation, Resources, Writing – review & editing, Visualization, Supervision, Project administration, Funding acquisition. **Douglas E. Wolfe:** Conceptualization, Investigation, Resources, Writing – review & editing, Supervision, Project administration, Funding acquisition. **Fan Ren:** Conceptualization, Formal analysis, Investigation, Writing – review & editing, Project administration, Funding acquisition. **Stephen Pearton:** Conceptualization, Formal analysis, Investigation, Writing – review & editing, Project administration, Funding acquisition.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

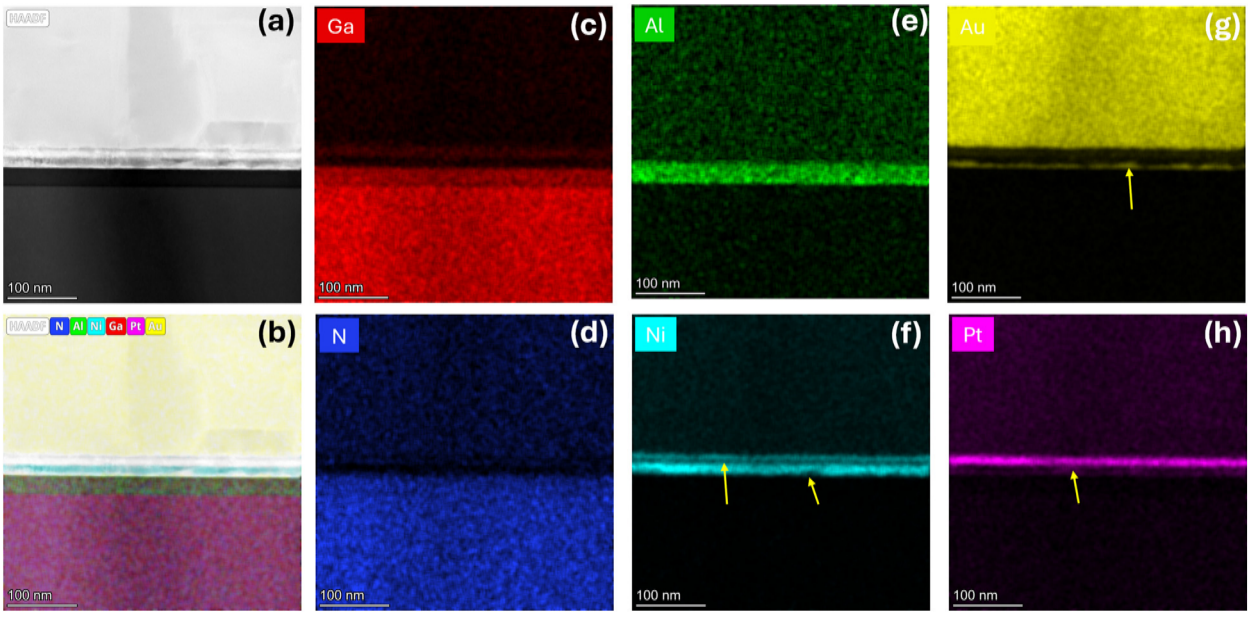

Fig. 9. EDS elemental mapping under the gate region after biasing at 4 V and 298 °C. (a) high angle annular dark field (HAADF) image. Elemental EDS maps of (b) all elements, (c) Ga, (d) N, (e) Al, (f) Ni, (g) Au, (h) Pt.

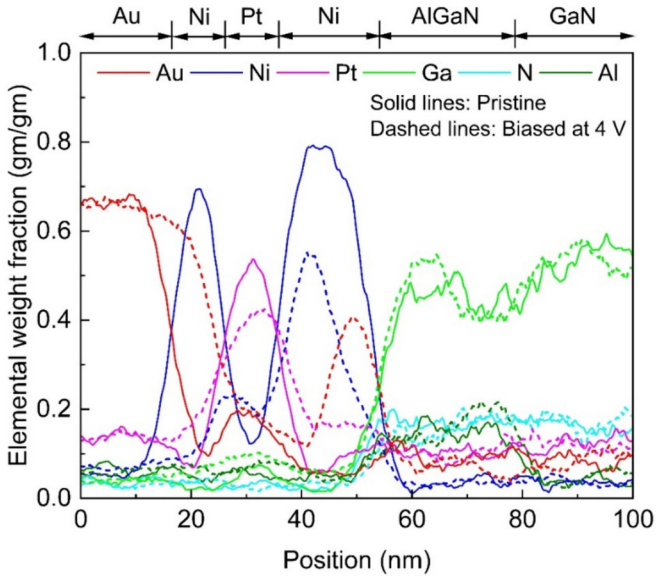

Fig. 10. Quantitative results of the EDS maps showing weight fraction of each element across the gate interface.

Data availability

The data that supports the findings of this study will be made available upon reasonable request.

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